

EMCR632/702 - Silicon Processes

Catalog: 0305-632 *Silicon Processes*
0305-702 *Microelectronics II*

Lecture#1

Introduction to Silicon Processes

Prof. K.D. Hirschman

9/6/10



Course Syllabus (1)

CATALOG: **EMCR632/702** **Silicon Processes**
 QTR: 20101 **Registration # 0305 632 / 702**

CREDITS: **EMCR632 - 4 credits**

PREREQUISITES: **EMCR350 / 701, EMCR460 & 560**

INSTRUCTOR: **Dr. Karl D. Hirschman, 17-2159, x5130, e-mail: kdhemc@rit.edu**

LAB ASSISTANTS: **Chris Shea, MicroE grad office 9-1360**

TEXTBOOK: **J.D. Plummer, M.D. Deal and P.B. Griffin, Silicon VLSI Technology –
 Fundamentals, Practice and Modeling, Prentice Hall, 2000.**

REFERENCES:

- **Wolf, Microchip Manufacturing, 2004**
- **Wolf & Tauber, Silicon Processing for the VLSI Era, Vol 1, 2nd Ed.**
- **Campbell, The Science and Engineering of Microelectronic Fabrication**
- **Wolf Vol 4, Submicron Process Technology, 2002**
- **Pierret, Semiconductor Device Fundamentals**
- **Various handouts, papers, etc.**



Course Syllabus (2)

COURSE DESCRIPTION & OBJECTIVES:

This is an advanced level course in silicon process technology. A detailed study of several of the individual processes utilized in the fabrication of VLSI circuits will be done, with a focus on engineering challenges such as shallow-junction formation and ultra-thin gate dielectrics. Front-end silicon processes will be investigated in depth including diffusion, oxidation, ion implantation, and rapid thermal processing. Particular emphasis will be placed on non-equilibrium effects. Device design and process integration details will also be emphasized. SUPREM-IV (Silvaco Athena) will be used extensively for process simulation. A project will involve the complete simulation of a twin-well CMOS process.

The laboratory will involve the fabrication and test of NMOS and PMOS transistors within the context of a full twin-well CMOS process. In addition, MOS capacitors and M-S contacts will be fabricated. Analysis of these devices will be done using I-V and C-V characterization. Silvaco process/device simulation will be used to model the twin-well CMOS process, and simulate device operation.



Course Syllabus (3)

TOPICS: Introduction and overview of IC processes & devices
- twin-well CMOS process flow

Process Technologies

- Impurity Diffusion in Si, atomistic model
- Thermal Oxidation of Si, Si/SiO₂ interface
- Ion Implant, Implant Damage & Annealing, TED
- Rapid Thermal Processing

Process Simulation (Silvaco Athena/Atlas)

Process Integration

SCHEDULE: Lecture: M,W,R 10-11AM 9-1129
Lab: T 9AM-noon 17-2510 (prelab)

GRADING PERCENTAGES:

Homework	10%
CMOS simulation project	10%
4 Quizzes (25min), drop lowest grade	30%
Comprehensive Final Exam	25%
Laboratory	25%

