Advanced CMOS Process Technology
Part 3

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OUTLINE

Introduction
Strained Silicon
FinFET’s
High-K, Metal Gate, Cu, Low-K
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INTRODUCTION

At ~0.1 µm gate length and smaller MOSFET performance is degraded so much that further scaling does not give improved performance of the integrated circuit as a whole.

Electrostatics (constant field scaling)
- D/S space charge layer is bigger part of device length L
- Vt rolloff, DIBL, channel length modulation (Lambda)
- Lower supply voltage means Lower threshold voltages implies larger off-current for given sub-Vt slope

Parasitics
- Gate Oxide Leakage implies larger on-currents
- Higher Source Drain series resistance implies lower Idrive
- Gate Depletion reduces Idrive and gm

Channel Transport – High channel doping reduces Idrive and gm
- Current Drive proportional to mobility
- Transconductance proportional to mobility

STRAINED SILICON

deeper, strains appear

Intel's move to strained silicon at 90 nm has industry scrambling to react

By David Lammers

AUSTIN, TEXAS – Intel Corp.'s announcement last week that it is adding strained silicon to its 90-nm technology mix stunned analysts and sent competitors into catch-up mode. One analyst, Dan Hutcheson of VLSI Research Corp., predicted that Intel's surprise move to implement a form of strained silicon at the 90-nm node--slated to move into manufacturing next year exclusively on 300-mm wafers at three Intel fabs--will reverberate as widely as IBM's 1997 decision to implement copper interconnects at 180-nm design rules.

Senior technology managers at half a dozen companies said last week that they either have decided to add strained silicon to their technology mix or already have dedicated research teams working on the problem:
Strained silicon can increase carrier mobility

A simple way to think about strained silicon follows: Tensile strain causes the silicon atoms to be pulled further apart making it easier for electrons to move through the silicon. On the other hand moving the atoms further apart makes it harder for holes to move because holes require bound electrons to move from a silicon atom to a neighboring silicon atom in the opposite direction, which is more difficult if they are further apart. Thus tensile strain increases mobility in n-type silicon and compressive strain increases mobility in p-type silicon (devices).

Strain can be created globally or locally. Growing an epitaxial layer of silicon on a silicon/germanium substrate creates (global) biaxial tensile strain in the silicon. N-MOSFETS built on these wafers will have higher mobility. P-MOSFETS will have lower mobility. Local strain can be created for each transistor such that N-MOSFETS see tensile strain and P-MOSFETS see compressive strain improving both transistors mobility. Local strain techniques include capping layers and introducing Ge or C in the source/drain regions.
INTRODUCTION TO STRAINED SILICON

The piezoresistive effect was first reported in 1954 [1] and has been used in making sensors for years. The effect of strain on the mobility of electrons and holes in semiconductors is important in today's sensors and transistors.

CRYSTAL STRUCTURE

Diamond Lattice (Silicon)

Equivalent Planes (100), (010), etc. Directions <110>, <011>, etc.

Miller Indices (1/x,1,y,1/z) smallest integer set

(100) wafer <110> direction

(100) plane

(111) plane

PIEZORESISTANCE

Piezoresistance is defined as the change in electrical resistance of a solid when subjected to stress. The piezoresistivity coefficient is $\Pi$ and a typical value may be $1E^{-10}$ cm$^2$/dyne.

The fractional change in resistance $\Delta R/R$ is given by:

$$\frac{\Delta R}{R} = \Pi \sigma$$

where $\sigma$ is the stress in dyne/cm$^2$. 
SINGLE CRYSTAL DIFFUSED RESISTORS

The n-type wafer is always biased positive with respect to the p-type diffused region. This ensures that the pn junction that is formed is in reverse bias, and there is no current leaking to the substrate. Current will flow through the diffused resistor from one contact to the other. The I-V characteristic follows Ohm’s Law: \( I = \frac{V}{R} \)

Sheet Resistance \( \rho_s \sim \frac{1}{q\mu \text{ Dose}} \) ohms/square

EXPRESSION FOR RESISTANCE

\[
R = R_o \left[ 1 + \pi_l \sigma_{xx} + \pi_T (\sigma_{yy} + \sigma_{zz}) \right]
\]

\[
R_o = \frac{(L/W)}{1/(q\mu(N,T) \text{ Dose})}
\]

\( \pi_l \) is longitudinal piezoresistive coefficient
\( \pi_T \) is transverse piezoresistive coefficient
\( \sigma_{xx} \) is the x directed stress
\( \sigma_{yy} \) is the y directed stress

Charles S. Smith
**PIEZORESISTANCE COEFFICIENTS**

In the <110> direction

<table>
<thead>
<tr>
<th></th>
<th>$\pi_L (E^{-11}/Pa)$</th>
<th>$\pi_T (E^{-11}/Pa)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrons</td>
<td>-31.6</td>
<td>-17.6</td>
</tr>
<tr>
<td>holes</td>
<td>71.8</td>
<td>-66.3</td>
</tr>
</tbody>
</table>

In the <100> direction

<table>
<thead>
<tr>
<th></th>
<th>$\pi_L (E^{-11}/Pa)$</th>
<th>$\pi_T (E^{-11}/Pa)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrons</td>
<td>-102</td>
<td>53.4</td>
</tr>
<tr>
<td>holes</td>
<td>6.6</td>
<td>-1.1</td>
</tr>
</tbody>
</table>

Tensile strain in (100) silicon increases mobility for electrons for flow in <110> direction.

Compressive strain in (100) silicon increases mobility for holes for flow in <110> direction.

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**PIEZORESISTANCE COEFFICIENTS VS DIRECTION**

For holes

- Piezoresistance coefficients at room temperature for the (001) plane of p-Si [2] Y. Kanda

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Charles S. Smith

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1. Mobility is affected by strain in semiconductors. Mobility can be increased or decreased depending on the type of strain (tensile, compressive) and the direction of strain relative to crystal orientation and current flow.

For (100) wafers and current flow in <110> direction:

2. Tensile strain n-type silicon enhances mobility of electrons. Tensile strain transverse to current flow enhances mobility of electrons.

3. Compressive strain in the direction of current flow in p-type silicon enhances mobility of holes. Tensile strain transverse to current flow enhances mobility of holes.
Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon–Carbon Source/Drain and Tensile-Stress Liner

Kuh-Wei Ang, Jing-Cheng Chai, Chih-Hung Tang, N. Balasubramaniam, Ming-Fu Li, Ganesh S. Samudra, and Yee-Chia Yeo

Abstract—We report the demonstration of 25-nm gate-length $L_{	ext{G}} = 0.025$-µm strained-Si MOSFETs featuring the silicon-carbon source and drain ($Si_{x-y}C_{y}$)/Si/SiO$_2$ regions and a thin-body thickness $T_{	ext{body}}$ of 18 nm. This is the smallest reported planar nMOSFET with the $Si_{x-y}C_{y}$/Si/SiO$_2$ structures. Strain-induced mobility enhancement due to the $Si_{x-y}C_{y}$/Si/SiO$_2$ leads to a significant drive-current $I_{	ext{Dmax}}$ enhancement of 65% over the control transistor. Furthermore, the integration of trench-stress SiN etch stop layer and $Si_{x-y}C_{y}$/Si/SiO$_2$ extends the $I_{	ext{Dmax}}$ enhancement to 87%. The performance enhancement was achieved for the devices with similar subthreshold swing and drain-induced barrier lowering. The $Si_{x-y}C_{y}$/Si/SiO$_2$ technology and its combination with the existing strained-Si technologies are providing for the future high-performance CMOS applications.

Index Terms—Electron mobility, nanosheetFET, silicon-carbon ($Si_{x-y}C_{y}$), silicon nitride layer, strain, stress.

I. INTRODUCTION

RECENTLY, channel-strain engineering is being actively pursued to enhance carrier mobility and drive current.

Fig. 1. (a) SEM image showing problems of silicon nitride during the high temperature (600°C) photolithography process. (b) Electron micrograph of $Si_{x-y}C_{y}$/Si/SiO$_2$ fully depleted structure with 25-nm gate-length $L_{	ext{G}}$. The physical gate length $L_{G}$ of 25 nm and the body thickness $T_{	ext{body}}$ of 18 nm. A SiN on-Si/SiO$_2$ etch with the tensile strain of 1.1% was used.

Fig. 2. (a) $I_{	ext{D}}$-$V_{	ext{GS}}$ characteristic of the control and strained nMOSFETs with single anneaux ($Si_{x-y}C_{y}$/Si/SiO$_2$) and dual anneaux ($Si_{x-y}C_{y}$/Si/SiO$_2$ and tensile-stress SiN/SiO$_2$). Significant $I_{	ext{Dmax}}$ enhancement of 57% is observed in the single anneaux nMOSFET and the control transistor. Even higher $I_{	ext{Dmax}}$ improvement of 67% is achieved with the integration of high stress SiN, and $Si_{x-y}C_{y}$/Si/SiO$_2$. (b) Single and dual anneaux strained devices are observed to enhance the transconductance by 65% and 139% over the control transistors, respectively.
IV. CONCLUSION

We demonstrated the successful integration of the Si$_{1-y}$Ge$_{y}$ S/D regions in the strained SOI nMOSFETs with the 25-nm gate lengths, enhancing the $I_{D_{max}}$ by 52%. Excellent subthreshold characteristics are achieved by the aggressive scaling of the SOI body thickness. Strain effects and $I_{D_{max}}$ are enhanced further by combining the high stress ESL and the Si$_{1-y}$Ge$_{y}$S/D stressors. Further performance boost can be achieved with an increased Si$_{1-y}$Ge$_{y}$S/D elevation.

Silicon SOI wafers with bi-axial tensile strain
BI-AXIAL STRAIN

Impact of Enhanced Mobility on Drive Current
Mobility Enhancement in Strained Si Channel/Relaxed SiGe n-MOSFETs

- Biaxial strain increases electron mobility above the universal MOS curve
- Mobility enhancements $\rightarrow I_p$ and $g_{m}$ improvements at 100 nm channel length

THREE GATE TRANSISTORS

Intel peers through 3 gates at post-planar-CMOS world

By David Lenes

The Coming Thing in Transistors

Three gate transistors have superior performance due to lower parasitic capacitance.
TRIPLE-GATE TRANSISTOR

Intel details its triple-gate transistor structure

The drive currents are 446 uA/um for n-FinFET and 356 uA/um for p-FinFET respectively.

The peak transconductance of the FinFET is very high (633uS/um at 105 nm Lg), because the hole mobility in the (110) channel is enhanced.

Gate Delay is 0.34 ps for n-FET and 0.43 ps for p-FET respectively at 10 nm Lg.

The subthreshold slope is ~60 mV/dec for n-FET and 101 mV/dec for p-FET respectively.

The DIBL is 71 mV/V n-FET and 120 mV/V for p-FET respectively.

Qin Zhang, 04/19/2005
20 nm gate length fin FETS used in worlds smallest flash memory cell.

Possible future chips with capacity of 32 Gbit.
1. Fin FETS have higher gm and Idrive because mobility is increased with lower doped channels.
2. Fin FETs have higher sub-threshold slope.
3. Fin FETS have lower DIBL

HIGH-K, METAL GATES, Cu, LOW-K, STRAINED Si

(HK+MG) from top chipmakers including Intel and IBM, as well as NEC, Toshiba, and Samsung.
HIGH-K FOR GATES

In its approach, “TI will leverage a chemical vapor deposition (CVD) process to deposit hafnium silicon oxide (HfSiO), followed by a reaction with a downstream nitrogen plasma process to form HfSiON or hafnium silicon oxynitride. By implementing the nitrided CVD technique, TI is able to solve the leakage issue without degradation of the other key parameters that customers have come to expect from SiO2-based gate dielectrics,” according to the company. “Through a modular addition to the typical CMOS gate stack process, HfSiON integration has been demonstrated offering mobility that is 90 percent of the silicon dioxide universal mobility curve, with effective oxide thicknesses (EOTs) below 1-nm,” according to TI.

EE Times, June 2007

HIGH K, METAL GATE

Parasitics: Gate Electrode Depletion

- Gate Electrode Depletion:
  - Lower inversion charge density
effectively limits EOT scaling

- Solution:
  - metal gates (high carrier density)
  - may also assist with high k
mobility issues

- Gate stack considered as a complete package:
  - Channel, dielectric, electrode

From: Dr. Judy Hoyt
MIT

R. Chau, et al.,
Intel, Nov. 2003
Electrostatics (constant field scaling)
- D/S space charge layer is a bigger part of device length L
- Vt rolloff, DIBL, channel length modulation (Lambda)
  (Fin FETs reduce effect of D/S space charge regions)
- Lower supply voltage means lower threshold voltages
  implies larger off-current for given sub-Vt slope
  (Increase sub-Vt slope with FINFETs)

Parasitic
- Gate Oxide Leakage implies larger on-currents (High K gate)
- Higher Source Drain series resistance implies lower Idrive
  (Schottky Metal Drain and Source)
- Gate Depletion reduces Idrive and gm (Metal gate)

Channel Transport – High channel doping reduces Idrive and gm
- Current Drive proportional to mobility
- Transconductance proportional to mobility
  (Increase mobility with strained silicon, higher mobility materials)
ADVANCED LITHOGRAPHY

Immersion Lithography
Optical Proximity Correction (OPC)
Phase Shift Masks
Off Axis Illumination
Resist Trimming
Double Exposure

Pixelated Phase Shift Mask

OPTICAL PROXIMITY CORRECTION (OPC)
1. The lithography process window for a typical pattern, a DRAM isolation layer, can be improved by using an optimized illuminator customized for that layer. In this example, NA=0.8, λ=248 nm and CD=120 nm.

2. It is possible to optimize both mask layout and illumination simultaneously — called source-mask optimization (SMO) — to maximize image contrast.
IMMERSION LITHOGRAPHY

- Increases NA
- Increased Resolution

DOUBLE PATTERNING

- IEEE Spectrum, Nov 2008
- Page 49
DOUBLE EXPOSURE

Double Exposure: 25nm gate features – arguably the physical limit of CMOS! – printed by MIT Lincoln Lab with a 0.60NA KrF stepper (Canon FPA-3000EX4). Source: MIT Lincoln Lab.

RESIST TRIMMING

- Resolution limit of Canon i-line stepper ~ 0.5 μm
- 1250 Å of PR is etched off each side of 0.5 μm PR lines in O₂ plasma to make 0.25 μm lines

Recipe Parameters:
- Power = 100 W
- Pressure = 400 mTorr
- O₂ = 20 sccm
- Gap = 1.65 cm
- Tool = LAM490

- PR Horizontal Etch Rate = 555 Å/min
- PR Vertical Etch Rate = 720 Å/min
- Anisotropy = (1-FR/Linux/FL) = 0.23
**GENEROUS DESIGN RULES**

- Active poly
- 90nm
- Generous 45nm
- Fully Scaled 45nm

**ADVANCED PACKAGING**
THROUGH WAFER VIAS

High Density Through Wafer Via Technology

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ABSTRACT

The Through Silicon Via (TSV) process developed by Texas Instruments is a through wafer connection as small as 50 μm thick silicon. TSVs via process enables MEMS design with significantly reduced size and true “White Level Packaging” — because they are completely hidden in consumer electronic applications. The TSV technology also enables integration of advanced interconnect functions in optical, biologic, sensors and microfluidic devices. With several printing companies using the process today and an extraordinary line-up of potential users, TSVs also make the process a candidate for the next generation of high density, high density microelectronics. The benefits of this technology will be facilitated by reasonable processing operations and high quality. An integrated, guided wafer bonding process and process in more detail on the several solutions made available by this enabling technology.

CHIP SCALE PACKAGE
C4 FLIP CHIP

Flip chip has the highest density of interconnects. Example: P2SC single-chip RISC 6000 processor has 2050 C4 bumps on 18x18 mm.

REFERENCES

6. EE Times Newsletter
8. UBM Tech Insights
### REVIEW QUESTIONS

1. Explain why steep sub-threshold slope is good for transistors in IC’s with millions of extremely small transistors?

2. Explain why mobility is lower in extremely small transistors?

3. What are the implications of lower mobility in extremely small transistors on overall integrated circuit performance?

4. What determines drive current? Why is it adversely affected in extremely small transistors? What can be done to improve drive current?