BJT IC Design

Dr. Lynn Fuller
Webpage: http://people.rit.edu/lffeee/
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035

Email: Lynn.Fuller@rit.edu
MicroE webpage: http://www.rit.edu/microelectronic/
OUTLINE

- Differential Amplifier
- Biasing, Current Sources, Mirrors
- Output Stages
- Operational Amplifiers
- References
- Homework Questions
DIFFERENTIAL AMPLIFIER

DC Analysis – assume:
Identical transistors,
Re=infinte, vin1=vin2=0

Then
Ic1=Ic2=Ie/2
Vo1=Vo2=Vcc-Rc Ie/2

Example: If Ie = 6mA
Vcc = 10, Vee = -10 and
Rc = 2K
Assume Vin1 = Vin2 = 0
Vo1 = Vo2 = 4.0 volts
VE = -0.7
VCE = 4.7
SMALL SIGNAL ANALYSIS

Lets define:
Differential input voltage
\[ vid = vi_1 - vi_2 \]
Common input voltage
\[ vic = (vi_1 + vi_2)/2 \]
Differential Output Voltage
\[ Vod = Vo_1 - Vo_2 \]
Common output voltage
\[ Voc = (Vo_1 + Vo_2)/2 \]
Single sided output voltage
\[ Voss = Vo_1 \text{ or } Vo_2 \]
VOLTAGE GAINS: \( Avd, Avc, \text{CMRR} \)

Differential mode voltage gain, \( Avd = \frac{Vod}{vid} \)

Let \( vin1 = \frac{vid}{2} + vic \) and \( vin2 = -\frac{vid}{2} + vic \)

\[
\begin{align*}
Ib1 &= \frac{(vin1 - Ve)}{r\pi} \\
Ib2 &= \frac{(vin2 - Ve)}{r\pi} \\
Ib1 &= \frac{(vid/2 - Ve)}{r\pi} \\
Ib2 &= \frac{(-vid/2 - Ve)}{r\pi}
\end{align*}
\]

\[
\begin{align*}
Vo1 &= -\beta \, ib1 \, Rc \\
Vo2 &= -\beta \, ib2 \, Rc \\
Vod &= Vo1 - Vo2 = -\beta \, ib1 \, Rc - -\beta \, ib2 \, Rc \\
Vod &= (\beta \, Rc / r\pi) \, (vid/2 + vid/2)
\end{align*}
\]

\[
Avd = -\frac{\beta \, Rc}{r\pi} = -gm \, Rc
\]
VOLTAGE GAINS: \( Avd, Avc, \text{ CMRR} \)

Common Mode Voltage Gain \( Avc = \frac{Voc}{Vic} = \frac{(Vo1 + Vo2)/2}{(vin1 + vin2)/2} \)

Let \( \text{Vid} = 0 \) thus \( \text{vin1} = \text{vin2} = \text{Vic} \)

\[ Ve = 2 \, Re \, (\beta +1) \, ib \]
\[ ib = \frac{(Vic - Ve)}{r\pi} \]

\[ ib = \frac{Vic - 2 \, Re \, (\beta+1)ib}{r\pi} \]  \( \text{Rearranging;} \)

\[ ib = \frac{Vic}{2 \, Re \, (\beta+1) + r\pi} \]

\[ Voc = \frac{-\beta \, ib1 \, Rc + -\beta \, ib2 \, Rc}{2} \]

Thus \( Voc = -\beta \, Rc \, ib = \frac{-\beta \, Rc \, Vic}{2Re \, (\beta+1) + r\pi} \)

\[ Avc = \frac{Voc}{Vic} = \frac{-\beta \, Rc}{2Re \, (\beta+1) + r\pi} \]
**OTHER RESULTS**

Single Sided Output Differential Voltage Gain:

\[
\frac{V_{oss}}{V_{id}} = \frac{1}{2} - \frac{\beta \ R_c}{r \pi}
\]

(Note: half)

Single Sided Output Common Mode Voltage Gain:

\[
\frac{V_{oss}}{V_{ic}} = \frac{-\beta \ R_c}{2 \ R_e (\beta+1) + r \pi}
\]

(Note: same)

Common Mode Rejection Ratio: CMRR is a figure of merit used to compare differential amplifiers

\[
CMRR = \frac{A_{vd}}{A_{vc}}
\]

Differential Mode Input Resistance:

\[
R_{id} = 2 \ r \pi
\]

Common Mode Input Resistance:

\[
R_{ic} = r \pi + (\beta+1) \ 2 \ R_e
\]
VARIATIONS

Variations:
1. Resistor between emitter and –Vee rather than current source
2. Series base resistors
3. Emitter resistors
4. Various types of current sources
5. Darlington configuration
6. FET’s
7. Single sided outputs
8. Active loads
9. unbalanced or non symmetrical circuits
EXAMPLE DIFFERENTIAL AMPLIFIER

Analyze the following differential amplifier, $\beta=200$
DC Analysis:

Small Signal Analysis:

Hand Calculation:
\[ Avd = \frac{1}{2} \text{gm} \ \text{Rc} \ \frac{rpi}{(1K+rpi)} = 62 \]
or
\[ Avd = \frac{1}{2} \beta \text{Rc} / (rpi + 1K) = 62 \]
SUMMARY

1. The differential amplifier should amplify the difference between the two input voltages.
2. The differential amplifier should suppress signals that are common to both inputs.
3. The differential amplifier with a constant current source is superior to the differential amplifier with just a resistor.
4. The common mode rejection ratio is used as a figure of merit for comparison.
5. The differential amplifier is a dc amplifier as well as an ac amplifier.
709 OPERATIONAL AMPLIFIER

Figure 5.21 Circuit layout for the 709 operational amplifier, (Photo: Fairchild.)

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741 OPERATIONAL AMPLIFIER

Figure 5.23: Photomicrograph of the 741 operational amplifier. Die size: 56 mils are. (Photo: Fairchild.)
SIMPLIFIED 741 OP AMP SCHEMATIC
**SIMPLE CURRENT SOURCE**

\[ I_e = \frac{(V - 0.7)}{R} \]

In the next few pages we will investigate current sources, level shifting and output stages of op amps.
CURRENT SOURCE (HW Problem 1)

There are many types of current sources. Consider the following:

What is $I_e$? (Ans: 1mA)

$Re_e = \infty$ if $ro = \infty$ (not there)

$Re_e$ is calculated by students in pro.1.

$Re_e$ in this example is 4.68 Meg

if $\beta = 100$ and $ro = 100K$
CURRENT SOURCES

\[ V_{be1} = V_{be2} + I_2 R_e \]

\[ \frac{KT}{q} \ln \frac{I_1}{I_s} = \frac{KT}{q} \ln \frac{I_2}{I_s} + I_2 R_e \]

\[ \frac{KT}{q} \ln \left( \frac{I_1}{I_2} \right) = I_2 R_e \]

Note: \( I_2 \) is always smaller than \( I_1 \)

\( I_e \) can be small without \( R_1 \) being small

\( R_{ee} \) is \( \sim \) Meg ohms
EXAMPLES FOR CURRENT SOURCE

Example 1: suppose $I_1 = 1 \text{ mA}$ and $I_2$ is $10 \text{ uA}$ find $R_e$

$$\frac{K_T}{q} \ln \left( \frac{I_1}{I_2} \right) = I_2 R_e$$

$$0.026 \ln \left( \frac{1\text{ mA}}{10\text{ uA}} \right) = 10\text{ uA} R_e$$

$$0.1197 = 10\text{ uA} R_e$$

$$R_e = 11.97K$$

Example 2: suppose $I_1 = 1 \text{ mA}$ and $R_e = 20K$ find $I_2$

$$\frac{K_T}{q} \ln \left( \frac{I_1}{I_2} \right) = I_2 R_e$$

$$0.026 \ln \left( \frac{1\text{ mA}}{I_2} \right) = 20K$$

Try $I_2 = \frac{\text{Left Side}}{20K}$

<table>
<thead>
<tr>
<th>$I_2$</th>
<th>Left Side</th>
</tr>
</thead>
<tbody>
<tr>
<td>1uA</td>
<td>179K</td>
</tr>
<tr>
<td>5uA</td>
<td>27.6K</td>
</tr>
<tr>
<td>6uA</td>
<td>22.2K</td>
</tr>
<tr>
<td>7uA</td>
<td>18.4K</td>
</tr>
<tr>
<td>Etc.</td>
<td></td>
</tr>
</tbody>
</table>
MORE CURRENT SOURCES

$$I_o = \frac{I_{ref}}{(1+2/\beta)}$$  $$I_o = \frac{I_{ref}}{(1+2/\beta^2)}$$  $$I_o = \frac{I_{ref}}{(1+2/\beta^2)}$$

Figure 1. (a) Basic, (b) Current-buffered, and (c) Wilson current sources.

Ree = ro  
Ree = ro  
Ree = MEG ohms
LEVEL SHIFTING

It would be nice to have zero volts out when we have zero volts in. We can achieve this by adding a level shifting stage.

\[
\begin{align*}
V_{cc} &= +10 \\
V_{ee} &= -10 \\
V_{o1} &= +10 \\
V_{o2} &= +10 \\
I_1 &= 6mA \\
R_c &= 2K \\
V_{o2} &= 4 \text{ volts} \\
\text{Thus we need a} & \quad 4 \text{ volt shift to make} \\
V_{out} &= 0 \text{ volts}
\end{align*}
\]

Note: in the ac equivalent circuit current sources are open circuits and voltage sources are short circuit. (We could use a battery)
Voltage sources should have constant voltage and zero source resistance.

\[ V_L = nV_{be} \]

\[ r_o = n\left(\frac{KT}{q}\right)/I_1 \]

\[ \frac{dV_L}{dT} = \frac{dV_z}{dT} + \frac{dV_{be}}{dT} \]
What is the purpose of D1?
(answer: reduces the change in VL with temperature)

Assume Ib is small compared to I1

\[ VL = VB - 0.7 \]

\[ VB - 0.7 = (V-0.7) \frac{R2}{R1+R2} \]

Therefore:

\[ VL = \frac{(V-0.7) R2}{R1+R2} \]

\[ ro = r_i + \frac{R1}{R2} \frac{1}{(\beta+1)} \]

Note: small
VOLTAGE MIRROR

+V

VZ

Load

Load

+V

multiple emitter transistor

VZ

Load

Load
LEVEL SHIFTING

\[ I_2 = \frac{V_{be}}{R_2} \]

\[ V_L = V_{be} \left( 1 + \frac{R_1}{R_2} \right) \]
LEVEL SHIFTING

It would be nice to have zero volts out when we have zero volts in. We can achieve this by adding a level shifting stage.

\[ V_{out} \]

\[ V_{shift} \]

\[ I_1 \]

\[ R_c = 2K \]

\[ I_e = 6mA \]

\[ V_{out} = 0 \text{ volts} \]

Thus we need a 4 volt shift to make \( V_{out} = 0 \) volts.
LEVEL SHIFTING

Level shifting should have high input resistance so it will not “load” the previous stage. Common collector input for high input resistance.

\[
VL = V_{be} \left(1 + \frac{R_1}{R_2}\right)
\]
OUTPUT STAGES

An output stage is needed to provide the capability of sourcing or sinking “large” currents to the load.

For $V_2 > 0.7$ $T_1$ is on and current flows from $+V$ thru $T_1$ and $RL$ to Gnd. $T_2$ is off.

For $V_2 < 0.7$ $T_2$ is on and current flows from Gnd thru $RL$ and $T_2$ to $-V$. $T_1$ is off.

With no signal in the transistors $T_1$ and $T_2$ are biased in an off state. This is called a class B amplifier.
OUTPUT STAGES

To eliminate the crossover distortion we can bias the transistors T1 and T2 so that they are just ready to conduct (ie Vbe ~ 0.65)

\[
\text{I}_1 = \frac{(2 \text{ V} - 1.4)}{2\text{R}_L} + \text{V_T1} + \text{Vin} + \text{V_L}
\]

Note: D1 and D2 are probably transistors identical to T1 and T2 with Base and Collector shorted. Thus I1 = I2 and is called the idle current. I1 = \((2 \text{ V} - 1.4)/2\text{R}\)
OUTPUT STAGES

Level shifting and output stage biasing

Output stage and load
When $T_1$ is on $I_L$ flows from $+V$ thru $T_1$, $Re$ and $R_l$ to Gnd. If $RL$ accidently went to zero $I_L$ would only go to $0.7/Re$ because at that value of $I_L$ $T_3$ would turn on which would remove the base drive from $T_1$ thus $I_L$ would be limited to $0.7/Re$. Similar for $T_2$. 
Design involves selecting values for RB and Re.
ACTIVE LOADS

Replacing some of the resistors with current sources requires less space and enables higher differential voltage gain and lower common mode gain because $r_o$ replaces $RC$ in the collector.

\[ r_o = \frac{V_A}{I_C} \]

Practically: $I/2$ sources cannot be made exactly correct. (see next page)
ACTIVE LOADS – CURRENT MIRROR

DC Analysis:
1. IE is constant current.
2. \( I_1 = I_2 = IE/2 \)

3. \( V_{o1} = V - 0.7 \)  
   actually \( V_{o1} = V - \frac{KT}{q} \ln \frac{I_1}{I_S} \)

4. \( V_{o2} = V - V_{EB1} - V_{BC2} \)  
   \( V_{o2} = V - \frac{KT}{q} \ln \frac{I_1}{I_S} - V_{BC2} \)

When \( V_{in1} = V_{in2} = 0 \) and \( I_1 = I_2 = IE/2 \)  
we have everything balanced and \( V_{BC2} = V_{BC1} = 0 \) thus \( V_{o2} = V - 0.7 \)

5. When \( V_{in1} > V_{in2} \) then \( I_1 > I_2 \) and \( V_{o2} \) rises toward \(+V\)
Note: p-p signal swing is about 1 volt
Let $V_1, V_2$ and $V_3$ be node voltages at node 1, 2 and 3, summing currents KCL

at node 1

$(\beta+1)(V_{in1}-V_1)/r\pi 1 + (V_2-V_1)/ro_1 + (V_3-V_1)/ro_2 + (\beta+1)(V_{in2}-V_1)/r\pi 2 - V_1/REE = 0$

at node 2

$V_2/rd + V_2/r\pi 4 + (V_2-V_1)/ro_1 + \beta(V_{in1}-V_1)/r\pi 1 = 0$

at node 3

$\beta V_2/r\pi 4 + V_3/ro_4 + (V_3-V_1)/ro_2 + \beta(V_{in2}-V_1)/r\pi 2 = 0$
SMALL SIGNAL ANALYSIS OF DIFF AMP WITH ACTIVE LOAD

Rearranging:

at 1
\[
\left(-\frac{1}{\text{REE}}-(\beta+1)/r\pi 1-1/\text{ro1}-1/\text{ro2}-(\beta+1)/r\pi 2\right)V_1+\left[1/\text{ro1}\right]V_2+\left[1/\text{ro2}\right]V_3 = \text{RHS}
\]

RHS = \(-V_{\text{in}2}(\beta+1)/r\pi 2 -V_{\text{in}1}(\beta+1)/r\pi 1\)

at 2
\[
[1/\text{ro1}-(\beta/r\pi 1)]V_1+[1/\text{ro4+1/r}\pi 4+1/\text{ro1}]V_2+0V_3 = -\beta V_{\text{in}1}/r\pi 1
\]

\(a_2\) \hspace{1cm} \(a_3\)

at 3
\[
[-\beta/r\pi 2-1/\text{ro2}]V_1+\beta/r\pi 4V_2+\left[1/\text{ro4+1/ro2}\right]V_3 = -\beta V_{\text{in}2}/r\pi 2
\]

\(a_4\) \hspace{1cm} \(a_5\)
SMALL SIGNAL ANALYSIS OF DIFF AMP WITH ACTIVE LOAD

Using Cramer’s rule and determinants

\[
V3 = \frac{-\text{Vin}_2(\beta+1)/r\pi_2 - \text{Vin}_1(\beta+1)/r\pi_1}{a_1 \quad 1/\text{ro}_1 \quad [-\beta\text{Vin}_1/r\pi_1] \\
               a_2 \quad a_3 \quad -\beta\text{Vin}_2/r\pi_2}
\]

\[
V3 = \frac{1/\text{ro}_3}{a_1 \quad 1/\text{ro}_1 \quad 1/\text{ro}_3 \\
               a_2 \quad a_3 \quad 0} \\
               a_4 \quad \beta/r\pi_4 \quad a_5
\]
SMALL SIGNAL ANALYSIS OF DIFF AMP WITH ACTIVE LOAD

Example: let \( r_{o1} = r_{o2} = r_{o4} = 50K \)
\( r_{p1} = r_{p2} = r_{p4} = 2K \)
\( \beta = 100, \quad r_d = 20, \quad R_E = \text{infinite} \)

a) If \( V_{in1} = 1/2 \) volt and \( V_{in2} = -1/2 \) volt
Find \( V_3 = 1246 \)
Therefore \( A_{vd} = 1246 \)

b) If \( V_{in1} = 1 \) volt and \( V_{in2} = 1 \) volt
Find \( V_3 = 0.00005108 \)
Therefore \( A_{vc} = 0.00005108 \)

c) \( \text{CMMR} = 1246/0.00005108 = 2.44e7 \)

Simple Hand Calculation:
\( A_{vd} = \frac{1}{2} \beta \frac{R_c}{r_{p}} = 1250 \)
or
\( A_{vd} = \frac{1}{2} \cdot g_m \frac{R_c}{r_{p}} = 1250 \)
LTSPICE SIMULATION

Note: SPICE model VA=100 for both

```plaintext
.measure tran Vout PP V(vout)
.measure tran Vindiff PP (V(vin1))
.measure Gain param (Vout/vindiff)

2N3906  Q4
2N3906  Q3
2N3904  Q1
2N3904  Q2

V1
SINE(0 100u 1k 0)
.tran 6m

Vout
10
-10
V+
V-

R1 50k
I1 6mA

Circuit: * C:\Users\lfee\Desktop\Old Desktop\SPICE FILES\LT SPICE
Direct Newton iteration for .op point succeeded.

vout: PP(vout)=0.391412 FROM 0 TO 0.006
vindiff: PP(v(vin1))=0.000196473 FROM 0 TO 0.006
gain: (vout/vindiff)=1992.19
```
EXAMPLE FROM LAB

\[
V_{CC} = +12 \text{ V}
\]

\[
\begin{align*}
R_{C1} & : 10 \text{ k}\Omega \\
R_{C2} & : 10 \text{ k}\Omega \\
R_{C3} & : 10 \text{ k}\Omega \\
R_{E1} & : 10 \mu\text{F} \\
R_{E2} & : 10 \mu\text{F} \\
R_L & : 100 \Omega \\
Q_1 & : Q2N3904 \\
Q_2 & : Q2N3906 \\
Q_3 & : Q2N3906 \\
Q_4 & : Q2N3906 \\
Q_5 & : Q2N3906 \\
Q_6 & : Q2N3904 \\
Q_7 & : Q2N3906 \\
v_{id} & : 6 \text{ mA} \\
v_{vo} & : -12 \text{ V} \\
-v_{EE} & : -12 \text{ V}
\end{align*}
\]

See lab notes
REFERENCES

1. Sedra and Smith,
4. Analog Integrated Circuits, Gray and Meyers
HOMEWORK – BIPOLAR IC DESIGN

1. Derive the exact value of $\text{Ree}$ for the current source on page 16.
2. Design a $100 \mu\text{A}$ current source.
3. For the simple op amp shown on page 31
   a. let $\text{vin1} = \text{vin2} = \text{zero}$. Select values for $\text{Rc}$ and $\text{Rb}$ such that $\text{Vout} = \text{zero}$.
   b. What is the maximum load current before current limiting?
   c. Calculate the small signal differential voltage gain.
4. Do a SPICE analysis of the simple op amp on page 31. Show DC $\text{Vout}$ vs $\text{Vin}$ and Voltage Gain. Answer: Gain ~128
5. Do a SPICE analysis of the differential amplifier using active loads shown on page 33. Let $\text{V}=10$volts. Show DC $\text{Vout}$ vs $\text{Vin}$ and Gain. Answer: Answer: Gain ~2000
CURRENT SOURCE (HW Problem 1)

There are many types of current sources. Consider the following:

What is $I_e$? (Ans: $1 \text{mA}$)

$R_e$ = infinity if $r_o$ = infinite (not there)
$R_e$ is calculated by students in pro.1.
$R_e$ in this example is 4.68 Meg
if $\beta = 100$ and $r_o = 100K$
Analyze the following differential amplifier, $\beta=200$
DC analysis: if $V_{in1} = V_{in2} = 0$, $I_{C1} = I_{C2}$ and $I_{B1} = I_{B2}$

KVL: $I_B \cdot 1K + 0.7 + 2(\beta+1)I_B \cdot 2K - 10 = 0$

$I_B = \frac{9.3}{(1K+2(200+1))} \cdot 2K = 11.6\mu A$

$I_C = 200 \cdot I_B = 2.32\ mA$

$V_{CE1} = 10 - I_B \cdot 1K - 0.7 = 10.7$

$V_{CE2} = 10 - I_C \cdot 2K - 0.7 = 6.06$

$r_T = \frac{\beta V_T}{I_C} = \frac{200 \cdot 0.026V}{2.32\ mA} = 2.24K$
AC analysis:

\[
\text{Avdss} = \frac{1}{2} \frac{\beta R_c}{(r\pi + 1K)}
\]

or

\[
\text{Avdss} = \frac{1}{2} \frac{0.089 \times 2K}{2.24K/3.24K} = 61.7
\]

\[
\text{Voss} = -\frac{-\beta R_c}{2Re(\beta+1) + (r\pi + 1K)}
\]

\[
\text{CMMR} = 61.7 / .496 = 125
\]
Do the DC analysis of this circuit.

Find the small signal voltage gain \( \frac{V_{out}}{V_{in}} \), Input resistance and output resistance.

Beta = 100
VA = infinite

Class Examples
Class Examples

Beta=100, VA = very large.

1.1 Do the DC analysis of this circuit with Vs=zero. What is Vout (offset voltage)?

1.2 Calculate the voltage gain, Avmid.

1.3 What could be done to reduce the offset voltage and increase the gain at the same time?