The SPICE models below were obtained from measurements of the CD4007 chip. This chip is made by several different companies such as TI and Fairchild. The chip designs are slightly different and the fabrication process is different but the transistor characteristics are suppose to be close to the same.

We measure the \( I_d-V_{ds} \) family of curves, \( I_d-V_{gs} \) transfer curves for saturation and non-saturation operation and for different substrate voltages. We also measure the physical dimensions using a calibrated microscope (after etching away the black plastic package). The gate and field oxide thicknesses and junction depths are inferred from the manufacturers data sheets. For example if the device is suppose to go to 20 volts then the gate oxide needs to be at least 50nm in thickness. The SPICE model should be third generation BSIM3 for better circuit simulation results (convergence). DC sweeps require specifying parameters for \( L, W, \) NRD, and NRS. Transient simulation also require AD, AS, PD, and PS to be specified. Transient simulations are compared to ring oscillator measurements for verification of SPICE parameters.

This chip has many parasitic resistors and diodes (capacitors) that are there for electrostatic discharge (ESD) protection. Those components will effect the transient performance of circuits made with these chips.
CD4007UB Types

**CMOS Dual Complementary Pair Plus Inverter**

High-Voltage Types (20-Volt Rating)

- CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

**Features:**
- Standardized symmetrical output characteristics
- Medium Speed Operation — $t_{PHL}, t_{PLH} = 30 \text{ ns (typ.)}$ at 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C

**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply-Voltage Range</td>
<td>MIN.</td>
<td>MAX.</td>
</tr>
<tr>
<td>(For $T_A = \text{Full Package Temperature Range}$)</td>
<td>3</td>
<td>18</td>
</tr>
</tbody>
</table>

**DIMENSIONS AND PAD LAYOUT FOR CD4007UBH**

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^-3 inch).
This figure shows the parasitic diodes in the CD4007 chip. Each reverse biased diode represents a capacitance that should be included when doing SPICE transient analysis. The resistors along with the reverse biased diodes provide electrostatic discharge protection (ESD).
Measured Id-Vds Family of Curves for 5, 10 and 20 volt Operation
These measurements were made using HP4145 Semiconductor Parameter Analyzer.

NMOS at 5 Volts
PMOS at -5 Volts

NMOS at 10 Volts
PMOS at -10 Volts

NMOS at 20 Volts
PMOS at -20 Volts
Picture of the CD4007, Three PMOS, Three NMOS
From these measurements the conversion is 0.35 um/pixel
CD4007 Transistor L and W Measurements

PMOS L=10um, W=360um

NMOS L=10um, W=170um
*SPICE MODELS FOR RIT DEVICES AND LABS - DR. LYNN FULLER 8-17-2015

*LOCATION DR. FULLER'S COMPUTER
*and also at: http://people.rit.edu/lffeee
*
*-----------------------------------------------------------------------

*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=170u Ad=8500p As=8500p Pd=440u Ps=440u NRD=0.1 NRS=0.1
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=4E-8 XJ=2.9E-7 NCH=4E15 NSUB=5.33E15 XT=8.66E-8
+VTH0=1.4 U0= 1300 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=300 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-8 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*

*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=360u Ad=18000p As=18000p Pd=820u Ps=820u NRS=O.54 NRD=0.54
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-8 XJ=2.26E-7 NCH=1E15 NSUB=8E14 XT=8.66E-8
+VTH0=-1.65 U0= 400 WINT=1.0E-6 LINT=1E-6
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-8 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*-----------------------------------------------------------------------
PSPICE Circuit Schematic for Generating Id-Vds Family of Curves
Note: Specification of Model RIT4007N7, L, W, NRD and NRS

W = 170u
L = 10u
NRD = 0.1
NRS = 0.1
PSPICE Simulation Profile

DC Sweep
V2 from 0 to 5 in 0.01 Volt steps
V1 from 0 to 5 in 0.5 Volt steps

Include text file with SPICE model RIT4007N7

Set up plot to plot Id
Use same setup as Last plot each time SPICE is run
Overlay of PSPICE Simulated Id-Vds Curves and Measured Id-Vds Curves
Measured Curves made with Digilent Analog Discovery Module
Overlay of LTSPICE Simulated Id-Vds Curves and Measured Id-Vds Curves

Measured Curves made with Digilent Analog Discovery Module
Measured Curves made with Digilent Analog Discovery Module

LTSPICE Simulated Id-Vds Curves

Measured with HP4145

CD4007

PSPICE Simulated Id-Vds Curves
LTSPICE Simulated Id-Vds Curves and Measured Id-Vds Curves at 10 Volts

CD4007 NMOS at 10 Volts, slope 0.0479m, Xint -118
LTSPICE Simulated Id-Vds Curves and Measured Id-Vds Curves at 20 Volts

LTSPICE Simulation
Measured CD4007 PMOS at -5 Volts

CD4007

VD

-5.000  -4.000  -3.000  -2.000  -1.000  0.000

-5.000m  -1.000m  -2.000m  -3.000m  -4.000m
PSPICE Circuit Schematic for Generating Id-Vds Family of Curves
Note: Specification of Model RIT4007P7, L, W, NRD and NRS

CD4007 PMOS at -5 Volts

```
V1 0
V2 0
RIT4007P7
M2

.dc V2 0 -5 -.01 V1 0 -5 -0.5
.INC C:/SPICE/RIT_Models_For_LTSPICE.txt
l=10u w=360u ad=18000p as=18000p pd=820u ps=820u NRS=.054 NRD=0.054
```
CD4007 PMOS at 5 Volts
PSPICE Circuit Schematic for Generating Id-Vds Family of Curves

Note: Specification of Model RIT4007P7, L, W, NRD and NRS
Overlay of Measured and PSPICE Simulated CD4007 PMOS at 5 Volts
Measured CD4007 PMOS at -5 Volts
Measured CD4007 PMOS at -10 Volts
Measured CD4007 PMOS at -20 Volts

**Conditions:**
- **Swp:** SMU1
  - **Start:** 0.0000 V
  - **Stop:** -20.0000 V
  - **Step:** -0.2000 V
  - **Pts:** 101

- **Step:** SMU2
  - **Start:** 0.0000 V
  - **Stop:** -20.0000 V
  - **Step:** -2.0000 V
  - **Pts:** 11

- **Con:** SMU3
  - **Val:** 0.0000 V

**Fit #1:**
- **Type:** Cursor
- **Slp:** 0.2400m
- **Yint:** -0.0477
- **Xint:** 198.9017

**Fit #2:**
- **None**

**Cursors:**
- **X:**
  - 20.0000
  - 19.0000
- **Y:**
  - -0.0525
  - -0.0523

ICS: 10:27:46
01/13/2015
Ring Oscillator including 25pF to model internal ESD devices