SPICE Model for NMOS and PMOS FETs in the CD4007 Chip
Dr. Lynn Fuller 7-10-2020

The SPICE models below were obtained from measurements of the CD4007 chip. This chip is made by several different companies such as TI and Fairchild. The chip designs are slightly different and the fabrication process is different but the transistor characteristics are suppose to be close to the same.

The SPICE models should give DC characteristics such as IC-VCE family of curves that match measured curves. For AC simulation the spacing and slope of the curves in the IC-VCE family needs to match measured curves because the spacing is gm and 1/slope is the transistor small signal output resistance. If they are correct than amplifier voltage gains from SPICE and from measurements should match. Small signal ac frequency response, and other time related responses are based on the internal capacitance in the transistor SPICE models and need to be combined with the transistor parameters (sizes) such as L, W, Ad, As, Pd, Ps, nrs and nrd. If all of that is correct then simulation of circuits such as ring oscillators should match measured ring oscillator results.

In addition packaged MOSFETS often have additional Electro Static Discharge (ESD) components in the package between the input and output pins of the package and the MOSFETs and circuits in the package. These components should protect the devices and not change the DC characteristics however they do introduce more capacitance internally where used. these chips.

We need good SPICE models for the transistors inside the CD4007 Chip. This is what we came up with.

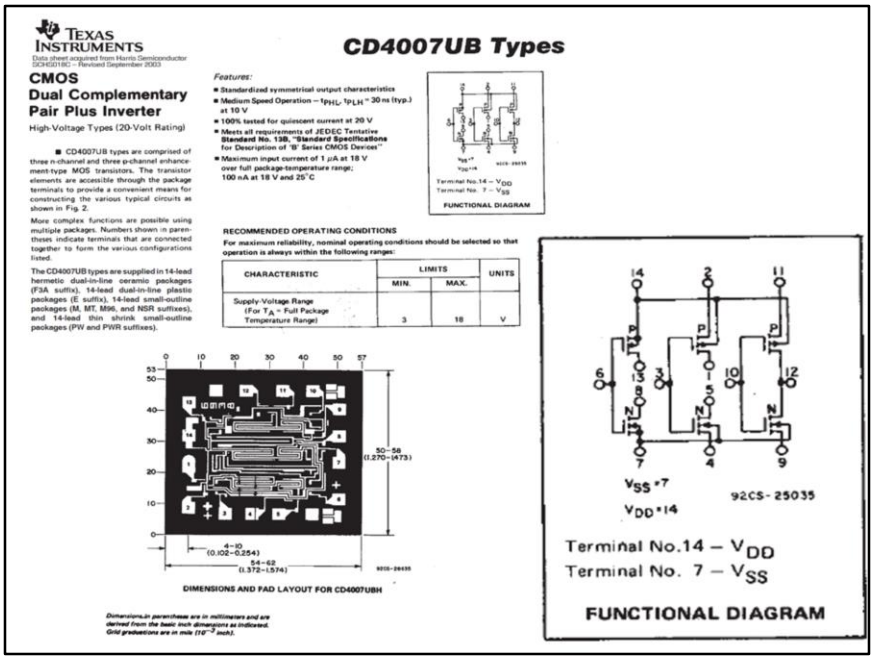
SPICE Model for NMOS and PMOS FETs in the CD4007 Chip
Dr. Lynn Fuller 8-17-2015

We hope to get SPICE model information from the manufacturer but that is not always possible. If not SPICE models can be created using manufacturers data sheets and measurements made on the devices.

We measure the Id-Vds family of curves, Id-Vgs transfer curves for saturation and non-saturation operation and for different substrate voltages. We also measure the physical dimensions using a calibrated microscope (after etching away the black plastic package). The gate and field oxide thicknesses and junction depths are inferred from the manufacturers data sheets. For example if the device is suppose to go to 20 volts then the gate oxide needs to be at least 50nm in thickness. The SPICE model should be third generation BSIM3 for better circuit simulation results (convergence). DC sweeps require specifying parameters for L, W, NRD, and NRS. Transient simulation also require AD, AS, PD, and PS to be specified. Transient simulations are compared to ring oscillator measurements for verification of SPICE capacitance parameters.

This chip has many parasitic resistors and diodes (capacitors) that are there for electrostatic discharge (ESD) protection. Those components will effect the transient performance of circuits made with these chips, such as ring oscillators.

We need good SPICE models for the transistors inside the CD4007 Chip. This is what we came up with.



TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS018C – Revised September 2003

CD4007UB Types

CMOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

■ CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation – t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C

FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

V_{SS} = 7
V_{DD} = 14
92CS-25035
Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}
FUNCTIONAL DIAGRAM

Starting with the Texas Instruments data sheet we find the pin out for this chip. The chip layout looks more complicated than just six MOSFETs. See next page.

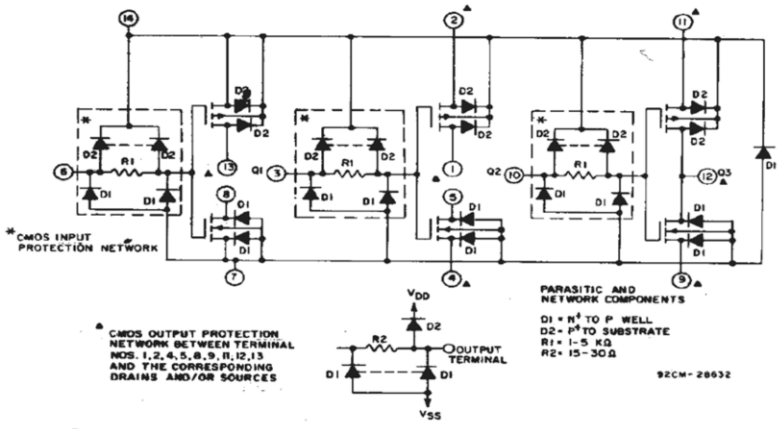
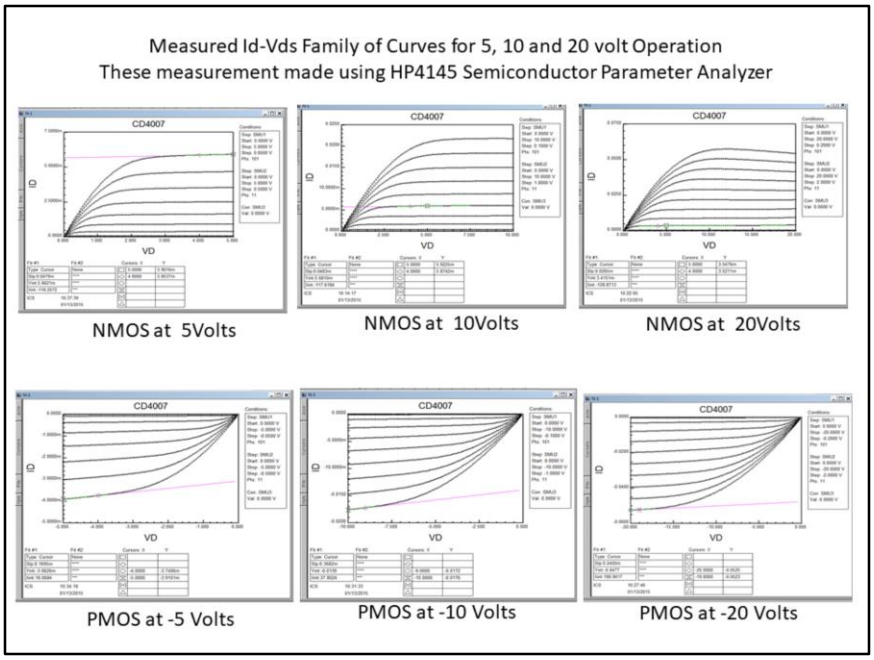


Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

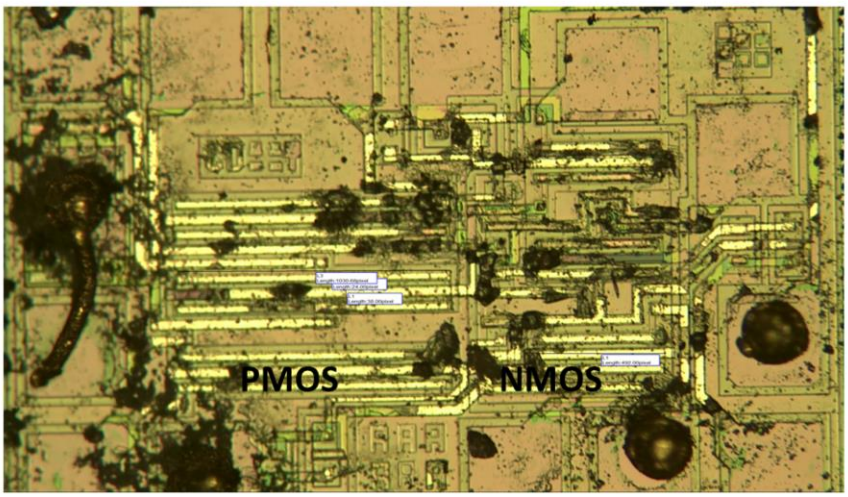
This figure shows the parasitic diodes in the CD4007 chip. Each reverse biased diode represents a capacitance that should be included when doing SPICE transient analysis. The resistors along with the reverse biased diodes provide electrostatic discharge protection (ESD).

The CMOS input protection circuitry is shown in the dotted box. For normal operation the input protection does not do much. It does add additional internal capacitance that will affect the speed of operation. Which will be important for circuits such as ring oscillators. If a voltage is applied to the input higher than the supply voltage or more negative than the negative supply value the diodes and resistors will safely dissipate the charge keeping the voltage to the gates lower than the breakdown voltage of the gate oxide.

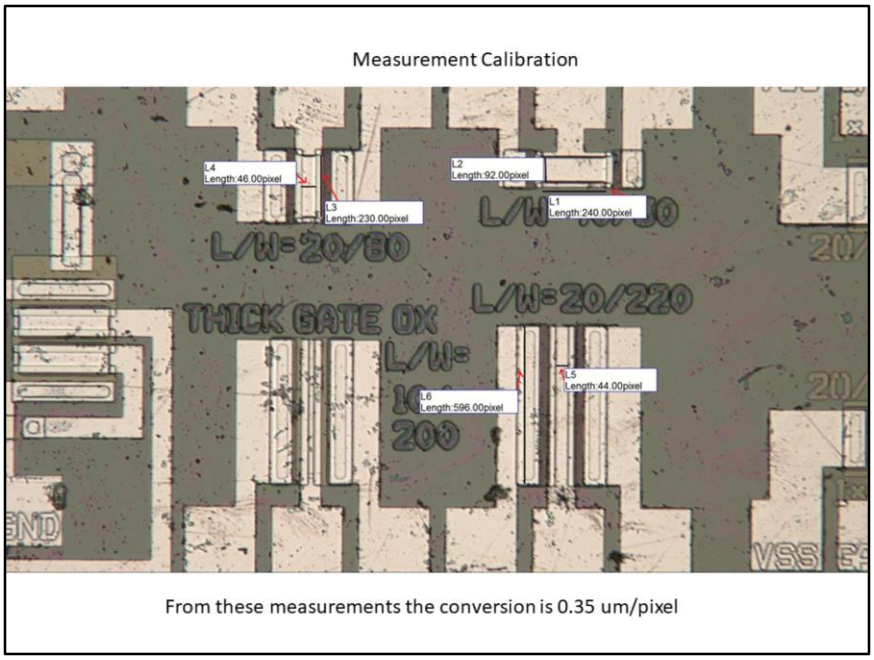


We started with measured ID vs VDS curves for 5, 10 and 20 volt operation. The data sheet indicate that these transistor max voltage is 18 Volts. They seem to work at 20 volts but the negative slope in the saturation region of the NMOS device at 20V indicates self heating which should be avoided. Our SPICE models should give matching current levels, slope and spacing of these curves.

Picture of the CD4007, Three PMOS, Three NMOS

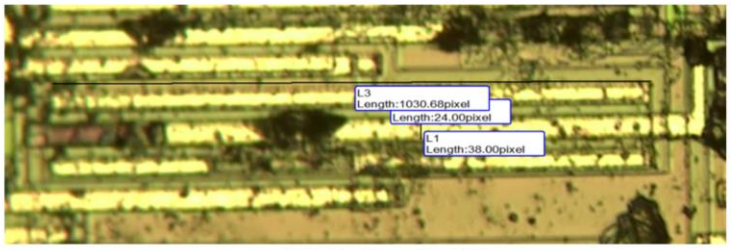


Next we wanted to get the actual L and W for the transistors. We etched off the plastic package and made measurements using an optical microscope. The measurement tool uses pixel counting to make the measurements. The measurements shown give W values of ~1000 pixel for the PMOSFET and ~500 pixel for the NMOSFET.

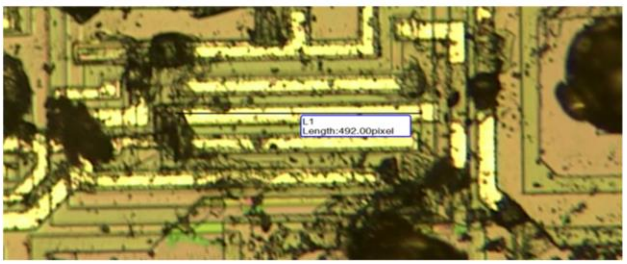


We made similar measurements for devices we designed and fabricated in the RIT laboratory. Since we know the L and W values. We computed a conversion of ~0.35um/pixel which we used to get the L and W measurements for the CD4007 transistors.

CD4007 Transistor L and W Measurements



PMOS L=10um, W=360um



NMOS L=10um, W=170um

Using the conversion of 0.35 um/pixel we came up with these L and W values. The area, perimeter and number of squares were estimated in a similar way. This measured L is probably not the real channel length depending on the fabrication details. L could be 5um depending the amount of lateral diffusion of the drain and source. Smaller L will give larger current and larger slope in the saturation region (smaller ro). Careful adjustment of SPICE model values and L is needed to match both DC current and ro to measured values. We found that L of 5 um gave better matching of ro.

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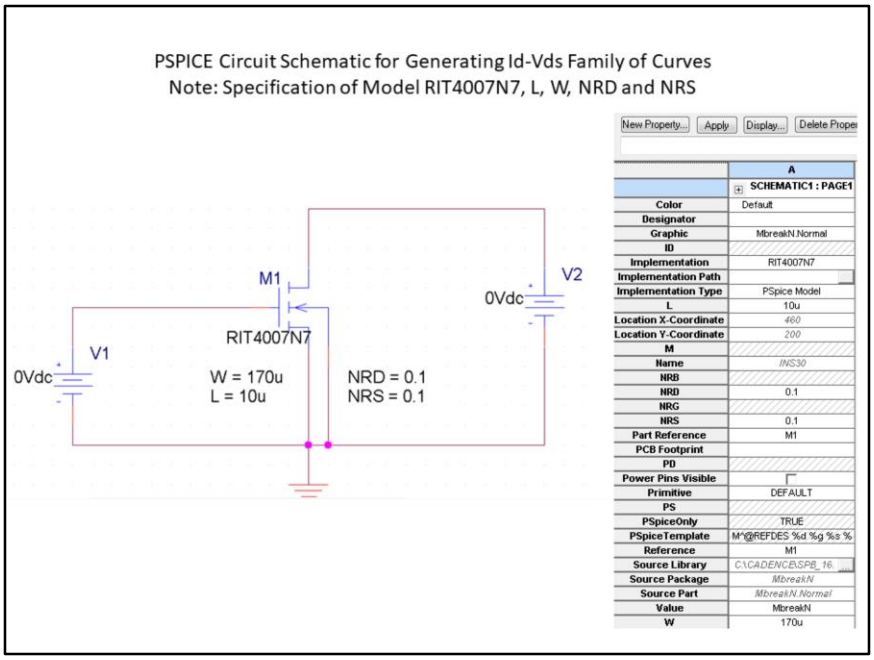
*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 7-10-2020
*LOCATION DR.FULLER'S COMPUTER
*and also at: http://people.rit.edu/lffeee
*Use notepad to edit text files, this file is RIT_Models_For_LTSPICE.txt
*
^----------------------------------------------------------------------
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=5u W=170u Ad=8500p As=8500p Pd=440u Ps=440u NRD=0.1 NRS=0.1
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=6E-8 XJ=2.9E-7 NCH=4E15 NSUB=5.33E15 XT=8.66E-8
+VTH0=1.4 U0= 925 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=200 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-8 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=5u W=360u Ad=18000p As=18000p Pd=820u Ps=820u NRS=0.54 NRD=0.54
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=6E-8 XJ=2.26E-7 NCH=3E15 NSUB=8E14 XT=8.66E-8
+VTH0=-1.65 U0= 225 WINT=1.0E-6 LINT=1E-6
+NGATE=5E20 RSH=800 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-8 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*----------------------------------------------------------------------
```

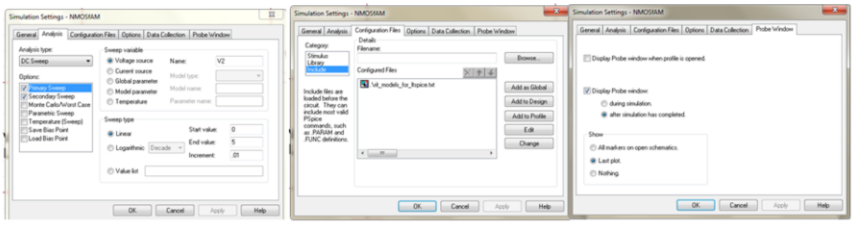
The MOSFET properties are shown in red. The SPICE mode is shown below the red text. To check if these models are close to correct we used SPICE to create ID vs VDS family of curves and compared the results with measured ID vs VDS family of curves.

Note: our pixel counting method for finding L and W seemed to be slightly off when generating SPICE curves and comparing to measured curves. Changing L to 5um seemed to give better results. The 5um adjustment in L is important. A similar 5um adjustment in W is ~1% … not so important. L is smaller that we see using the microscope due to diffusion under the gate from both sides… can not see without removing the gate material. What is important is to have the measured characteristics and SPICE generated characteristics match each other.



For DC sweeps we need the properties for L, W, NRD AND NRS and the SPICE model shown on the previous page.

PSPICE Simulation Profile

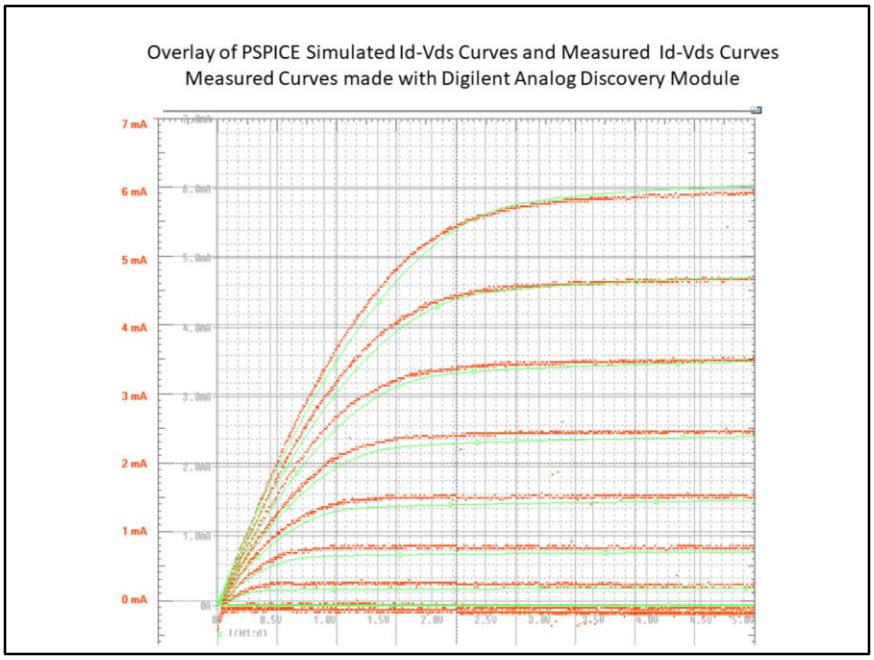


DC Sweep
V2 from 0 to 5 in 0.01 Volt steps
V1 from 0 to 5 in 0.5 Volt steps

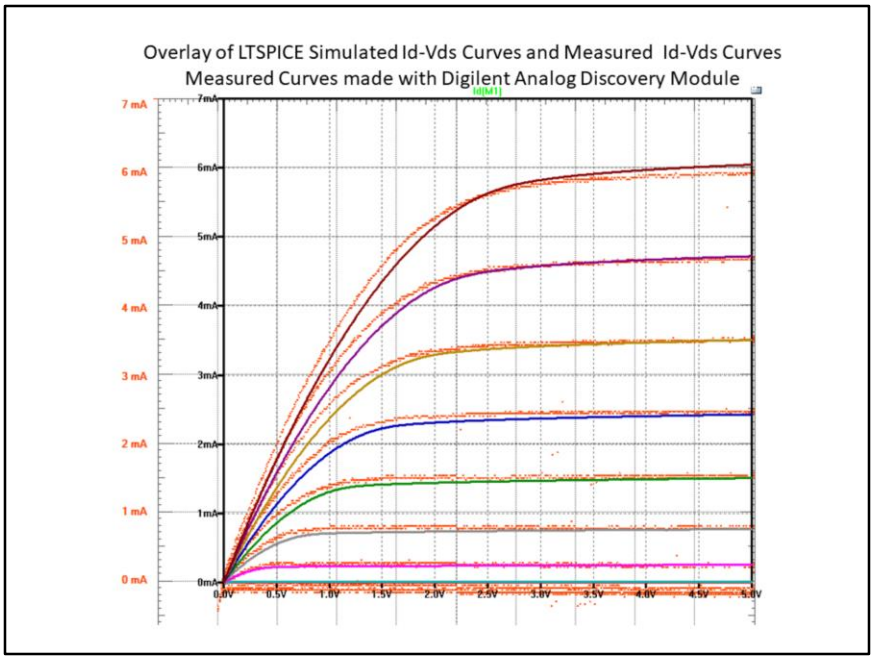
Include text file with
SPICE model RIT4007N7

Set up plot to plot Id
Use same setup as Last plot
each time SPICE is run

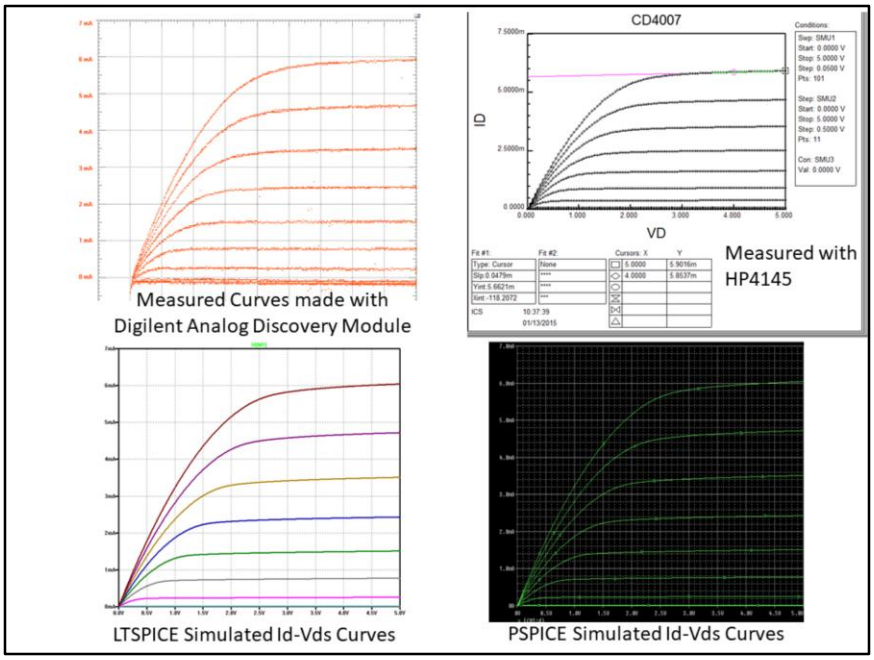
For Cadence PSPICE the DC sweeps and SPICE model text file location are set up in the simulation profile.



The red/orange curves are measured. The green curves are PSPICE simulated.

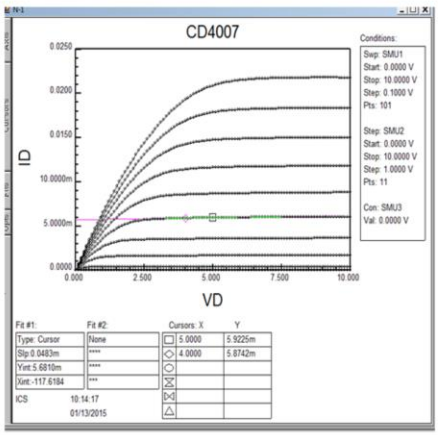


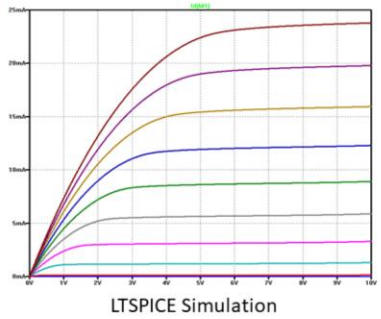
The red/orange curves are measured and the different color curves are LTSPICE simulated.



Since all of these overlay well then the SPICE model is close to good for the 0 to 5 volt VDS.

LTSPICE Simulated Id-Vds Curves and Measured Id-Vds Curves at 10 Volts



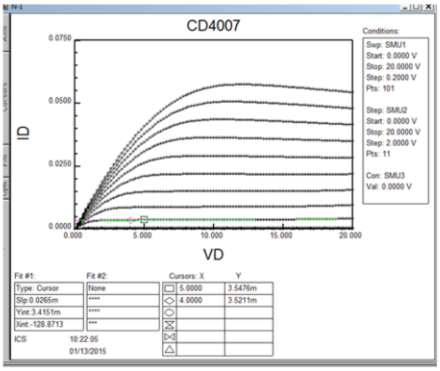


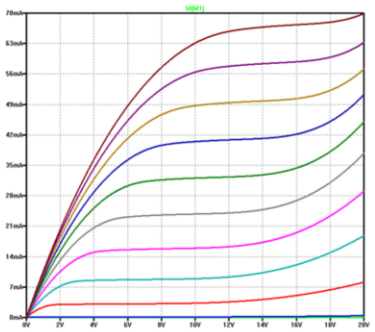
LTSPICE Simulation

CD4007 NMOS at 10 Volts, slope 0.0479m, Xint -118

At 10 volts VDS also good overlay

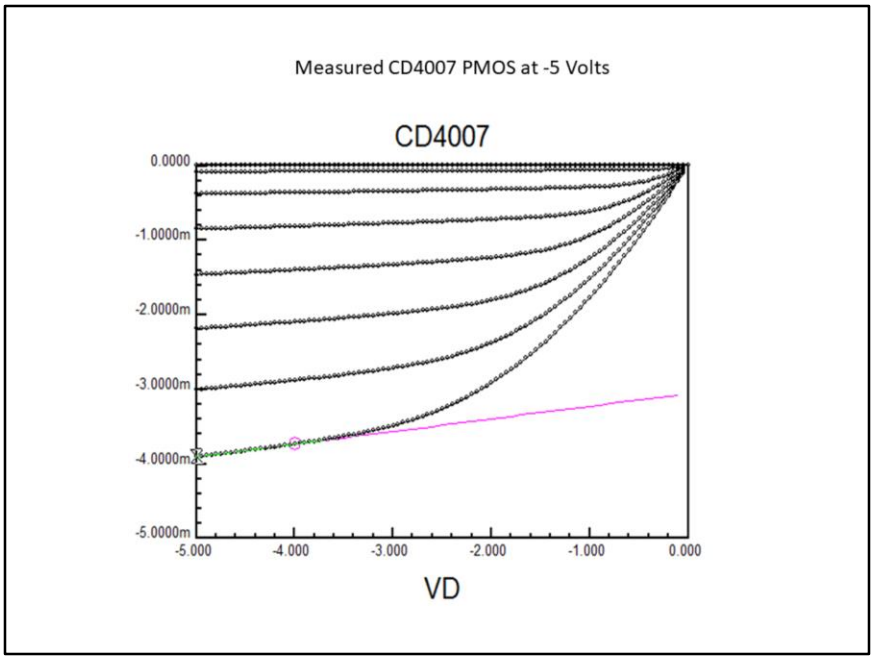
LTSPICE Simulated Id-Vds Curves and Measured Id-Vds Curves at 20 Volts





LTSPICE Simulation

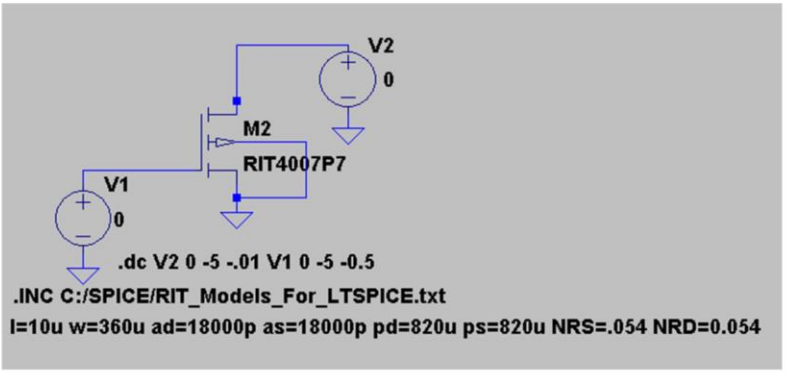
At 20 volts not so good overlay but the devices have 18 volt maximum according to the data sheet.



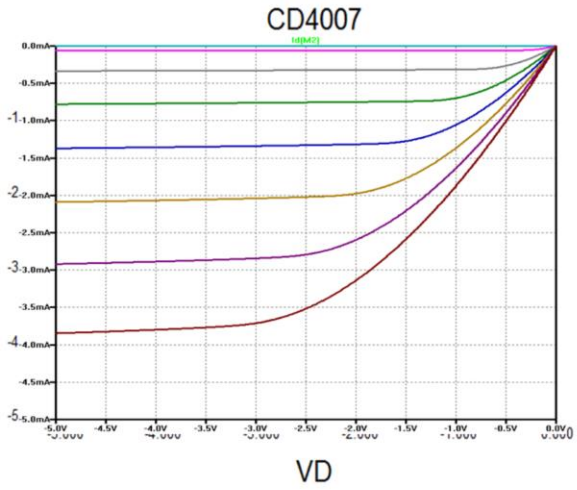
All of the above was also done for the PMOSFETs.

PSPICE Circuit Schematic for Generating Id-Vds Family of Curves
Note: Specification of Model RIT4007P7, L, W, NRD and NRS

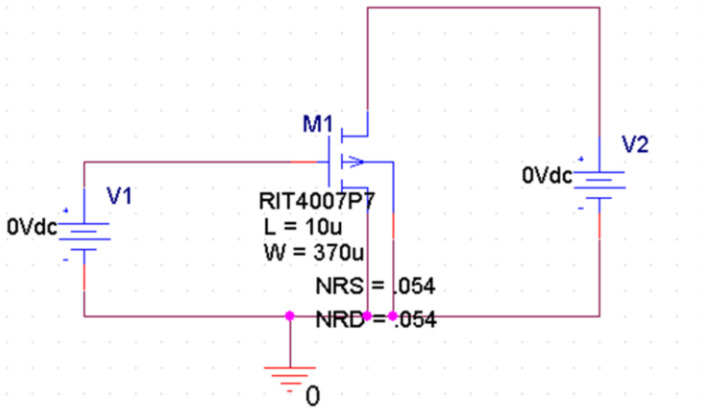
CD4007 PMOS at -5 Volts



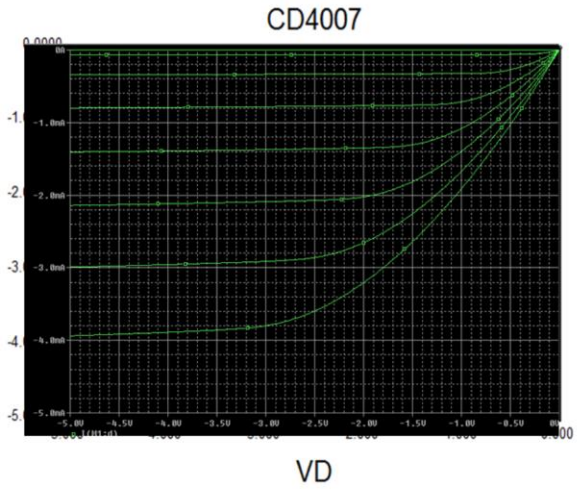
CD4007 PMOS at 5 Volts

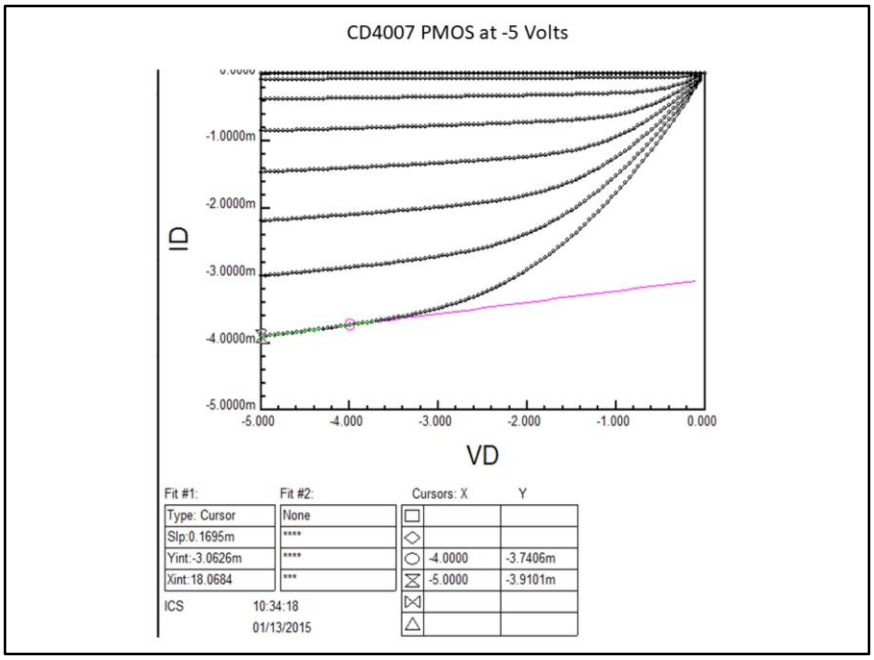


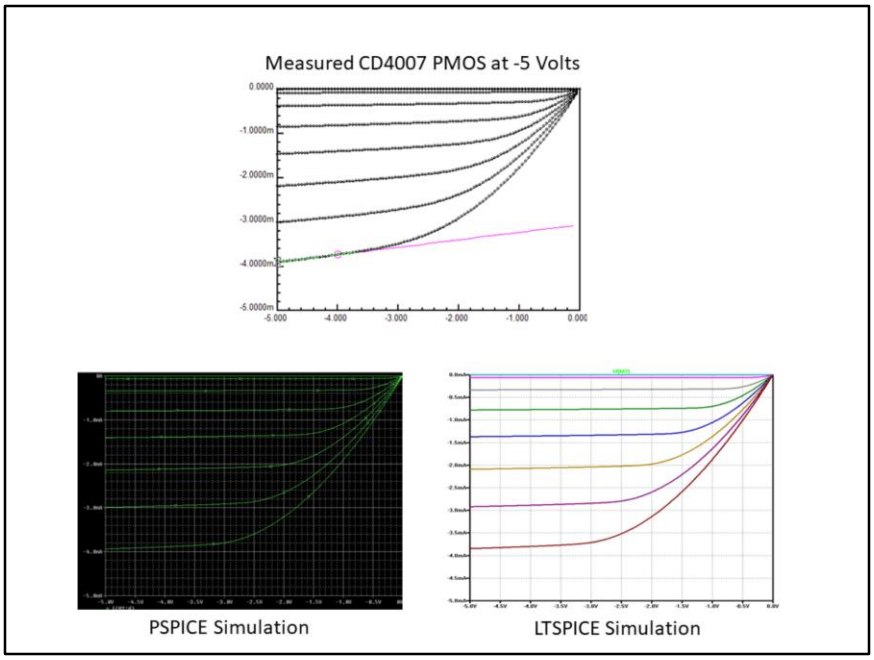
PSPICE Circuit Schematic for Generating Id-Vds Family of Curves
Note: Specification of Model RIT4007P7, L, W, NRD and NRS



Overlay of Measured and PSPICE Simulated CD4007 PMOS at 5 Volts

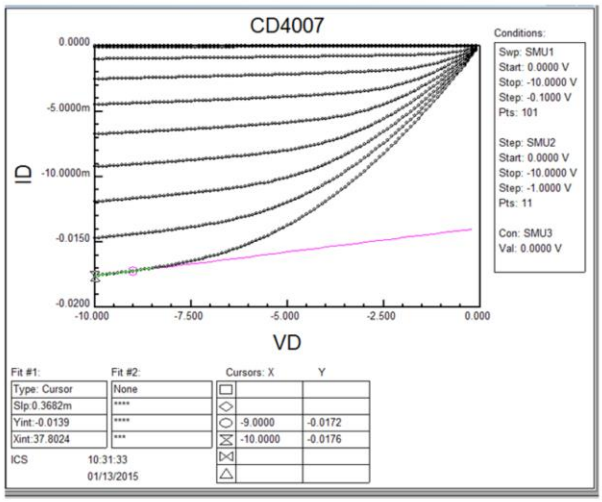



CD4007 PMOS at -5 Volts
-1.0000m
-2.0000m
-3.0000m
-4.0000m
-5.0000m
ID
-5.000
-4.000
-3.000
-2.000
-1.000
0.000
VD
Fit #1:
Type: Cursor
Slp:0.1695m
Yint:-3.0626m
Xint:18.0684
Fit #2:
None
****
****
***
ICS
10:34:18
01/13/2015
Cursors: X
Y
-4.0000
-3.7406m
-5.0000
-3.9101m

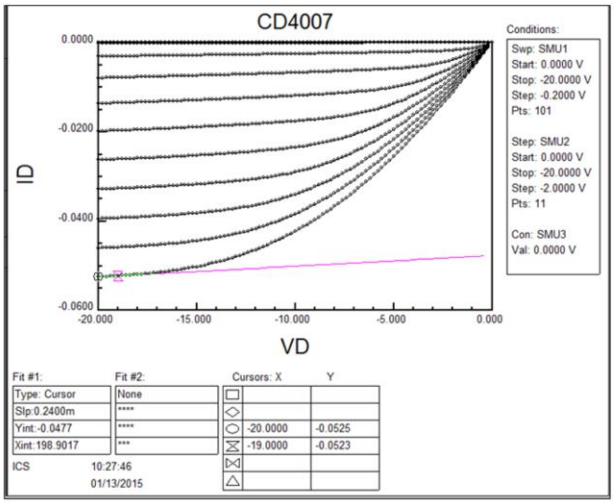


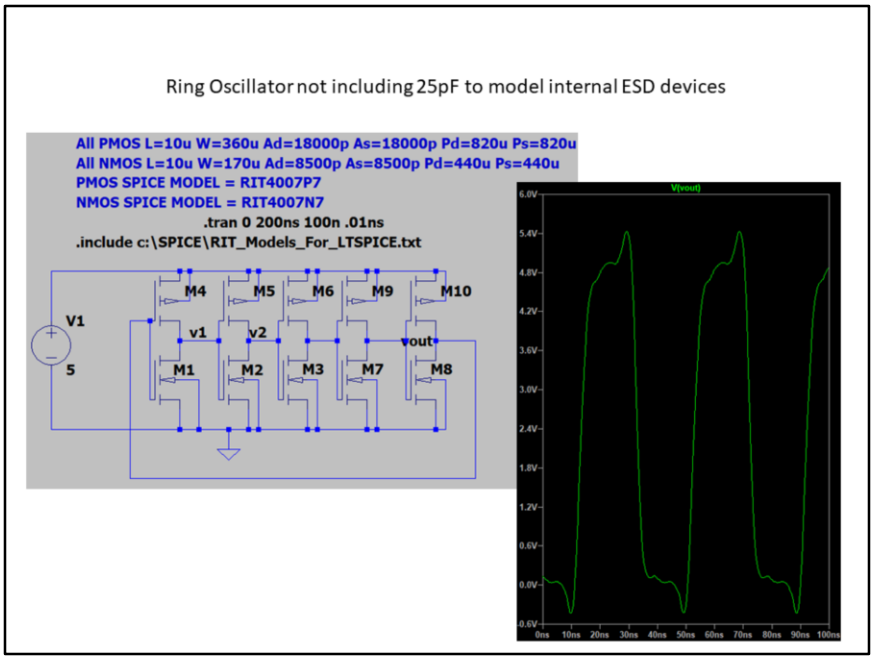
These measured and SPICE simulated curves overlay fairly well.

Measured CD4007 PMOS at -10 Volts



Measured CD4007 PMOS at -20 Volts





If the ring oscillator waveform matches with the simulation then the AC parameters such as Cj and Cjsw, etc. must be correct. SPICE will calculate the internal capacitance for each transistor using the properties and the SPICE model. However the capacitance of the input ESD protection circuitry needs to be added at each input as a separate capacitor to ground. This is the subject of a lab in Digital Electronics. That lab is posted on Dr. Fullers webpage.