CMOS Testing of First John Galt Chips

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10-25-2009 CMOSTestingJohnGalt1.ppt
OUTLINE

Introduction
Process Technology
Design Rules
Chip Floor Plan
Structures for Fabrication Process and Evaluation
Sensors
Digital Circuits
Analog Circuits
Projects
References
This document will describe a new CMOS test chip. The test chip will be used to develop CMOS process technology and to verify analog and digital circuit designs. In addition the test chip includes a variety of CMOS compatible sensors and signal processing electronics for those sensors. A section of the chip is for manufacturing process characterization and transistor parametric characterization. Other sections of the chip have basic digital and analog circuits, chip scale packaging designs and projects to evaluate various Microsystems architectures. For example a variable frequency oscillator, binary counter and shift register allows for capacitor sensor measurement and Blue-Tooth wireless transmission of data to a remote host. The test chip will be used with RIT’s SUB-CMOS and ADV-CMOS processes.
RIT Subµ CMOS

150 mm wafers
Nsub = 1E15 cm-3
Nn-well = 3E16 cm-3
Xj = 2.5 µm
Np-well = 1E16 cm-3
Xj = 3.0 µm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin= 1.0 µm
LDD/Side Wall Spacers
Vdd = 5 Volts, Vto= +/- 1 Volt
Two Layer Metal
**CMOS Testing of John Galt Chip**

**SUB-CMOS 150 CROSSECTION**

- NMOSFET
  - N+ Poly
  - N+ D/S
  - LDD
  - n+ well
  - Channel Stop

- PMOSFET
  - 5000 Å Field Oxide
  - LDD
  - p+ D/S
  - n+ well contact

**p-Type Substrate 10 ohm-cm**

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*Microelectronic Engineering*

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We will use a modified version of the MOSIS TSMC 0.35 2P 4M design rules. Eventually we hope to be compatible with MOSIS but new process technology needs to be developed at RIT to do that (PECVD Tungsten, improved lithography overlay, 4 layer metal). We plan to use one layer of poly and two layers of metal. We will use the same design layer numbers with additional layers as defined on the following pages for manufacturing/maskmaking enhancements. Many of the designs will use minimum drawn poly gate lengths of 2µm where circuit architecture is the main purpose of the design. Minimum size devices (Drawn Poly = 0.5µm, etc.) are included to develop manufacturing process technology.
**LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Ldrawn</td>
<td>min drawn poly length, 2λ</td>
<td>0.50µm</td>
</tr>
<tr>
<td>Lmask</td>
<td>? Depends on +/-bias</td>
<td>1.00µm x 5</td>
</tr>
<tr>
<td>Lpoly</td>
<td>Lresist after photo (resist trimming??)</td>
<td>0.50µm</td>
</tr>
<tr>
<td></td>
<td>Lpoly after poly etch</td>
<td>0.40µm</td>
</tr>
<tr>
<td></td>
<td>Lpoly after poly reoxidation</td>
<td>0.35µm</td>
</tr>
<tr>
<td>Lint</td>
<td>distance between junctions, including under diffusion</td>
<td>0.30µm</td>
</tr>
<tr>
<td>Leff</td>
<td>distance between space charge layers, Vd = Vs = 0</td>
<td>0.20µm</td>
</tr>
<tr>
<td>L</td>
<td>distance between space charge layers, when Vd = what it is</td>
<td>0.11µm</td>
</tr>
</tbody>
</table>

**Source at 0 V**

**Drain at 3.3V**

Internal Channel Length, \( L_{\text{int}} \) = distance between junctions, including under diffusion

Effective Channel Length, \( L_{\text{eff}} \) = distance between space charge layers, \( V_d = V_s = 0 \)

Channel Length, \( L \), = distance between space charge layers, when \( V_d = \) what it is

Extracted Channel Length Parameters = anything that makes the fit good (not real)
CMOS Testing of John Galt Chip

MOSIS TSMC 0.35 2POLY 4 METAL PROCESS


MOSIS SCmos Technology Codes and Layer Map

SCN4M and SCN4M_SUBM

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

SCN4M: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicided block and thick oxide option available only on the TSMC process.

SCN4M_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMI, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

<table>
<thead>
<tr>
<th>Layer</th>
<th>GDS</th>
<th>CIF</th>
<th>CIF Synonym</th>
<th>Rule Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>N WELL</td>
<td>42</td>
<td>CWN</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>ACTIVE</td>
<td>43</td>
<td>CAA</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>THICK ACTIVE</td>
<td>60</td>
<td>CTA</td>
<td></td>
<td>24</td>
</tr>
<tr>
<td>POLY</td>
<td>46</td>
<td>CPG</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>SILICIDE BLOCK</td>
<td>29</td>
<td>CSB</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>N PLUS SELECT</td>
<td>45</td>
<td>GSN</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>P PLUS SELECT</td>
<td>44</td>
<td>GSP</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>CONTACT</td>
<td>28</td>
<td>GCG</td>
<td>GCG</td>
<td>5, 6, 19</td>
</tr>
<tr>
<td>POLY_CONTACT</td>
<td>47</td>
<td>GGP</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>ACTIVE_CONTACT</td>
<td>48</td>
<td>GCA</td>
<td></td>
<td>6</td>
</tr>
<tr>
<td>METAL1</td>
<td>49</td>
<td>CM1</td>
<td>CMF</td>
<td>7</td>
</tr>
<tr>
<td>VIA</td>
<td>50</td>
<td>CV1</td>
<td>CVA</td>
<td>8</td>
</tr>
<tr>
<td>METAL2</td>
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<td>CM2</td>
<td>CMS</td>
<td>9</td>
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<td>VIA2</td>
<td>61</td>
<td>CV2</td>
<td>CV8</td>
<td>14</td>
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<td>METAL3</td>
<td>62</td>
<td>CM3</td>
<td>GMT</td>
<td>15</td>
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<td>VIA3</td>
<td>35</td>
<td>CV8</td>
<td>CV7</td>
<td>21</td>
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<td>METAL4</td>
<td>31</td>
<td>CM4</td>
<td>CMQ</td>
<td>22</td>
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<td>GLASS</td>
<td>52</td>
<td>COG</td>
<td></td>
<td>10</td>
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<tr>
<td>PADS</td>
<td>26</td>
<td>XP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Comments</td>
<td>--</td>
<td>CX</td>
<td></td>
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<table>
<thead>
<tr>
<th>Technology</th>
<th>Layers</th>
<th>Remarks</th>
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<tbody>
<tr>
<td>TSMC</td>
<td>0.35</td>
<td>0.25</td>
</tr>
<tr>
<td>0.35 micron</td>
<td></td>
<td>SCN4M</td>
</tr>
<tr>
<td>2P4M (4 Metal Polycided, 3.3 V/5 V)</td>
<td>Non-Fab layer used to highlight pads</td>
<td></td>
</tr>
</tbody>
</table>

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### MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

<table>
<thead>
<tr>
<th>MASK LAYER NAME</th>
<th>MENTOR NAME</th>
<th>GDS #</th>
<th>COMMENT</th>
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</thead>
<tbody>
<tr>
<td>N WELL</td>
<td>N_well.i</td>
<td>42</td>
<td></td>
</tr>
<tr>
<td>ACTIVE</td>
<td>Active.i</td>
<td>43</td>
<td></td>
</tr>
<tr>
<td>POLY</td>
<td>Poly.i</td>
<td>46</td>
<td></td>
</tr>
<tr>
<td>N PLUS</td>
<td>N_plus_select.i</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>P PLUS</td>
<td>P_plus_select.i</td>
<td>44</td>
<td></td>
</tr>
<tr>
<td>CONTACT</td>
<td>Contact.i</td>
<td>25</td>
<td>Active_contact.i 48 poly_contact.i 47</td>
</tr>
<tr>
<td>METAL1</td>
<td>Metal1.i</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>VIA</td>
<td>Via.i</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>METAL2</td>
<td>Metal2.i</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>VIA2</td>
<td>Via2.i</td>
<td>61</td>
<td>Under Bump Metal</td>
</tr>
<tr>
<td>METAL3</td>
<td>Metal3.i</td>
<td>62</td>
<td>Solder Bump</td>
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These are the main design layers up through metal two.
# More Layers Used in Mask Making

<table>
<thead>
<tr>
<th>Layer</th>
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<th>GDS</th>
<th>Comment</th>
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</thead>
<tbody>
<tr>
<td>cell_outline.i</td>
<td>70</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>alignment</td>
<td>81</td>
<td>Placed on first level mask</td>
<td></td>
</tr>
<tr>
<td>nw_res</td>
<td>82</td>
<td>Placed on nwell level mask</td>
<td></td>
</tr>
<tr>
<td>active_lettering</td>
<td>83</td>
<td>Placed on active mask</td>
<td></td>
</tr>
<tr>
<td>channel_stop</td>
<td>84</td>
<td>Overlay/Resolution for Stop Mask</td>
<td></td>
</tr>
<tr>
<td>pmos_vt</td>
<td>85</td>
<td>Overlay/Resolution for Vt Mask</td>
<td></td>
</tr>
<tr>
<td>LDD</td>
<td>86</td>
<td>Overlay/Resolution for LDD Masks</td>
<td></td>
</tr>
<tr>
<td>p plus</td>
<td>87</td>
<td>Overlay/Resolution for P+ Mask</td>
<td></td>
</tr>
<tr>
<td>n plus</td>
<td>88</td>
<td>Overlay/Resolution for N+ Mask</td>
<td></td>
</tr>
<tr>
<td>tile_exclusion</td>
<td>89</td>
<td>Areas for no STI tiling</td>
<td></td>
</tr>
</tbody>
</table>

These are the additional layers used in layout and mask making.
CMOS Testing of John Galt Chip

Other Layers

Design Layers
- N-WELL (42)
- ACTIVE (43)
- POLY (46)
- P-SELECT (44)
- N-SELECT (45)
- CC (25)
- METAL 1 (49)
- VIA (50)
- METAL 2 (51)

Other Design Layers
- P+ Resolution (87)
- STI Resolution (82)
- Stop Resolution (84)
- Vt Resolution (85)
- Active Resolution (83)
- N+ Resolution (88)

Layers:
- Nmos Vt
- Poly
- N+
- P+
- Active
- Stop

Dimensions:
- 81
- 43
- 46
- 85
- 84
- 87
- 42
- 49
- 45
- 25

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## MASK ORDER FORM

<table>
<thead>
<tr>
<th>Design Layer</th>
<th>Name</th>
<th>Mark Level Name</th>
<th>Number</th>
<th>Boolean Function</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>NWELL</td>
<td>1</td>
<td>n-well</td>
<td>42</td>
<td>(42 OR 81 OR 82) INVERT</td>
<td>Dark Field Mark</td>
</tr>
<tr>
<td></td>
<td></td>
<td>alignment</td>
<td>01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>n-well</td>
<td>02</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACTIVE</td>
<td>2</td>
<td>active-area-i</td>
<td>43</td>
<td>(43 OR 03)</td>
<td>Clear Field Mark</td>
</tr>
<tr>
<td></td>
<td></td>
<td>active-area-o</td>
<td>03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STOP</td>
<td>3</td>
<td>n-well</td>
<td>42</td>
<td>(42 OR 04)</td>
<td>Clear Field Mark</td>
</tr>
<tr>
<td></td>
<td></td>
<td>channel_step</td>
<td>04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMOSUT</td>
<td>4</td>
<td>p-plu_select-i</td>
<td>44</td>
<td>(44 OR 05)</td>
<td>Dark Field Mark</td>
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<tr>
<td></td>
<td></td>
<td>p-nar_vt</td>
<td>05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POLY</td>
<td>5</td>
<td>poly_i</td>
<td>46</td>
<td>None</td>
<td>Clear Field Mark, Bipolar 6*0.5μm</td>
</tr>
<tr>
<td>LDD-H</td>
<td>6</td>
<td>n-plu_select-i</td>
<td>45</td>
<td>(45 OR 06)</td>
<td>Dark Field Mark</td>
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<tr>
<td></td>
<td></td>
<td>LDD</td>
<td>06</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LDD-P</td>
<td>7</td>
<td>n-plu_select-i</td>
<td>44</td>
<td>(44 OR 06)</td>
<td>Dark Field Mark</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDD</td>
<td>06</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N+DS</td>
<td>9</td>
<td>n-plu_select-i</td>
<td>45</td>
<td>(45 OR 88)</td>
<td>Dark Field Mark</td>
</tr>
<tr>
<td></td>
<td></td>
<td>n-plu</td>
<td>08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P+DS</td>
<td>9</td>
<td>p-plu_select-i</td>
<td>44</td>
<td>(44 OR 87)</td>
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<tr>
<td></td>
<td></td>
<td>p-plu</td>
<td>07</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CC</td>
<td>10</td>
<td>contact</td>
<td>25</td>
<td>(25 OR 87 OR 47) INVERT</td>
<td>Dark Field Mark</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Active_contact</td>
<td>40</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Poly_contact</td>
<td>47</td>
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<td></td>
</tr>
<tr>
<td>METAL1</td>
<td>11</td>
<td>met+1</td>
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<td>None</td>
<td>Clear Field Mark</td>
</tr>
<tr>
<td>VIA</td>
<td>12</td>
<td>Via</td>
<td>50</td>
<td>INVERT</td>
<td>Dark Field Mark</td>
</tr>
<tr>
<td>METAL2</td>
<td>13</td>
<td>met+2</td>
<td>51</td>
<td>None</td>
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<tr>
<td>VIA2</td>
<td>14</td>
<td>Via2</td>
<td>61</td>
<td>None</td>
<td>Clear Field Mark</td>
</tr>
<tr>
<td>METAL3</td>
<td>15</td>
<td>met+3</td>
<td>62</td>
<td>None</td>
<td>Clear Field Mark</td>
</tr>
</tbody>
</table>

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CMOSTestchip2007
  Process
  Digital
  Primitive Cells
  Basic Cells
  Macro Cells
  Analog & Mixed
  Projects
  Packaging
  MEMS
  Project 1
  Project 2

Packaging Project

Packaging Project

Project 2 MEMS

Project 1

Analog and Mixed

Digital Macro Cells

Process & Manufacturing Structures

Sensors

Digital Cells

Alignment, Resolution, Overlay, Logo, Title

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The test chip is divided into nine cells each 5 mm by 5 mm. The cells are divided into 36 individual tiny cells each 800 µm by 800 µm in size plus 200 µm sawing streets. Most structures fit into the tiny cells including a 12 probe pad layout for probe card testing. The overall chip size is 14800 µm by 14800 µm plus 200 µm sawing street to give x and y step size of 15 mm by 15 mm.
CMOS Testing of John Galt Chip

ANALOG TO DIGITAL CONVERTER

Output Register
Comp
Ref Buf
Successive Approximation Register
DAC
CMOS Testing of John Galt Chip

**BIG NMOS AND PMOS FETS**

L/W = 100µm/150µm

Big enough for easy Nanospec Measurements
Not for device testing
NMOS Field Vt > 10 volts

PMOS Field Vt < -25 volts
CMOS Testing of John Galt Chip

NMOS AND PMOS TRANSISTORS

Various L/W Ratios

NMOS 2/8
PMOS 2/8
FULLY SCALED SUB MICRON TRANSISTORS
CMOS Testing of John Galt Chip

NMOS TEST RESULTS

2I４=LⅥ

Rochester Institute of Technology Microelectronic Engineering

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### NMOS Transistor Family of Curves

#### Conditions:
- **Swp:** SMU1
- **Start:** 0.0000 V
- **Stop:** 5.0000 V
- **Step:** 0.0833 V
- **Pts:** 61
- **Swp:** SMU2
- **Start:** 0.0000 V
- **Stop:** 5.0000 V
- **Step:** 0.5000 V
- **Pts:** 11
- **Con:** SMU3
- **Val:** 0.0000 V
- **Con:** SMU4
- **Val:** 0.0000 V

#### Results:
- **$I_{d \text{max}}$ at $V_{gs} = 5$ and $V_{ds} = 5$:** 0.4447 mA
- **$I_{ds \text{sat}}$ at $V_{gs} = 5$ and $V_{ds} = 4$:** 0.4422 mA
- **$\lambda$ (slope/$I_{ds \text{sat}}$):** 0.0061 V
- **$I_{\text{drive}}$:** 111 μA/μm

#### Dimensions:
- **Length $L$:** 2 μm
- **Width $W$:** 4 μm
NMOS Transistor $I_d$ vs $V_{gs}$ with $V_{ds} = 0.1$ volts

Conditions:
- Con. SMU1 Val: 0.1000 V
- Swp. SMU2 Start: 0.0000 V Stop: 5.0000 V Step: 0.0500 V Pts: 101

$gm_{max} = 0.008679 \, \text{mS}$
$X$ intercept = $V_T = 0.75 \, \text{V}$
$gm = \frac{2.17 \, \text{mS/mm}}{V}$
$VT = 0.75 \, \text{V}$
NMOS Transistor Subthreshold Plot at \( V_d = 0.1 \) and \( V_d = 5 \)

Measure in the Dark

- \( I_{\text{max}} @ V_{ds} = 0.1 \): 2.50E-05 A
- \( I_{\text{max}} @ V_{ds} = 5 \): 4.44E-04 A
- \( I_{\text{min}} @ V_{ds} = 0.1 \): 1.55E-12 A
- \( I_{\text{min}} @ V_{ds} = 5 \): 1.55E-12 A
- \( V_{gs} @ I_{d} = 10 \text{nA}, V_{d} = 0.1 \): 0.440 V
- \( V_{gs} @ I_{d} = 1 \text{nA}, V_{d} = 0.1 \): 0.320 V
- \( V_{gs} @ I_{d} = 1 \text{nA}, V_{d} = 5 \): 0.320 V
- \( I_{\text{on/off}} @ V_{ds} = 0.1 \): 7.21 DEC
- \( I_{\text{on/off}} @ V_{ds} = 5 \): 8.46 DEC
- Sub-threshold swing = 120 mV/DEC
- DIBL = 0.0 mV/V
NMOS Field Oxide FET, Id versus Vgs

X intercept = 10.0 V
Field VT = 10.0 V
Note: Vt adjust mask made incorrectly
Vt = ~ -2.0
### MOSFET EXTRACTED PARAMETERS

Lot Number = F080729 – Wafer Number = D2, Die Location R= , C=

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PMOS</th>
<th>NMOS</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>Mask Length / Width</td>
<td>2/4</td>
<td>2/4</td>
<td>µm</td>
</tr>
<tr>
<td>VT</td>
<td>-2.0</td>
<td>0.75</td>
<td>V</td>
</tr>
<tr>
<td>Lambda (for Vgs = Vdd)</td>
<td>0.018</td>
<td>0.006</td>
<td>V⁻¹</td>
</tr>
<tr>
<td>Max gm / mm of channel width</td>
<td>0.90</td>
<td>2.17</td>
<td>mS/mm</td>
</tr>
<tr>
<td>Idrive</td>
<td>33</td>
<td>111</td>
<td>µA/µm</td>
</tr>
<tr>
<td>Ion/Ioff @ Vd = 0.1V</td>
<td>7.47</td>
<td>7.21</td>
<td>Decades</td>
</tr>
<tr>
<td>Ion/Ioff @ Vd = 5V</td>
<td>8.52</td>
<td>8.46</td>
<td>Decades</td>
</tr>
<tr>
<td>Ioff @ Vd = 0.1V</td>
<td>3E-13</td>
<td>1.55E-12</td>
<td>A/µm</td>
</tr>
<tr>
<td>Ioff @ Vd = 5V</td>
<td>3E-13</td>
<td>1.55E-12</td>
<td>A/µm</td>
</tr>
<tr>
<td>Sub-Vt Slope @ Vd = 0.1V</td>
<td>99</td>
<td>120</td>
<td>mV/Dec</td>
</tr>
<tr>
<td>Sub-Vt Slope @ Vd = 5 V</td>
<td>99</td>
<td>120</td>
<td>mV/Dec</td>
</tr>
<tr>
<td>DIBL@1nA/µm = ∆Vg / ∆Vd</td>
<td>0</td>
<td>0</td>
<td>mV/V</td>
</tr>
<tr>
<td>Field VT</td>
<td>-25.2</td>
<td>10</td>
<td>V</td>
</tr>
</tbody>
</table>
RING OSCILLATORS AND SEM STRUCTURES

17 Stage Un-buffered Output  L/W=2/30 Buffered Output

L/W 8/16  4/16  2/16  73 Stage  37 Stage

SEM Structures  CMOS Inverter Crosssection
RING OSCILLATOR DESIGN

2µm gate length
5 Volt
73 stage
4x Buffer Output
1x Buffer Output
Unbuffered Output
RING OSCILLATOR RESULTS

17 Stage unBuffered
L=8μm
Frequency = 2MHz
Period = 500ns
\(td = 14\text{ns}\)

73 Stage 4X Buffer
L=2μm
Frequency = 4.37MHz
Period = 230ns
\(td = 1.58\text{ns}\)

These worked the others did not. Design errors in 2\textsuperscript{nd} & 3\textsuperscript{rd} wrong layer for CC, missing CC in 5\textsuperscript{th}
SEM CROSSSECTION OF MOSFET

NMOSFET  PMOSFET

P-well     N-well

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VAN DER PAUWS AND CBKR’s

NWELL  PWELL  N+       P+      N
-       -
POLY M1     M2

2µm M1toPoly  2µm M1toP+  4µm M1toPoly  4µm M1toP+
2µm M1toM2    2µm M1toN+  4µm M1toM2    4µm M1toN+
2µm M1toP+    2µm M1toN+  4µm M1toP+    4µm M1toN+
N-Well
Rhos=888 ohm/sq
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VAN DER PAUW TEST RESULTS

Metal 1
Rhos=0.0457 ohm/sq
Metal 2
Rhos=0.0615 ohm/sq
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SERPENTINES, COMBS, AND VIA CHAINS

To evaluate metal1, metal2, CC and Via layer quality.
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M1-M2 VIA CHAIN

F081201

M1-M2 Via chain with 512 Vias and total resistance of 118 ohms or 0.231 ohms per contact
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SENSORS

Interdigitated and Plate Capacitors
Diodes and Heaters
Resistors
Photovoltaic Cells, 1x, 2x, 4x
Two side by side pn diode sensors for differential readout
CAPACITORS

M2  M1  M1 to M2  M1 to Poly

120 Fingers gives ~0.3 pF  670µm/470µm Plate  ~3 pF
PARALLEL PLATE CAPACITORS

TEOS=4000Å

Measured = 22.5pF

Calculated = \( \varepsilon_0 \varepsilon_r \frac{\text{Area/d}}{d} \)

= \( (8.85 \times 10^{-14})(3.9)(670 \times 470)(1E-4)/(0.4) \)

= 27.2 pF

TEOS=5000Å

Measured = 29.4pF

Calculated = 22pF
METAL ONE INTERDIGITATED FINGER CAPACITORS

Measured: 1.1pF
Calculated: 2.3pF

120 fingers
3um line
3um space
Er = 4.9
Overlap = 440um

C = LN\left(\frac{4\pi\varepsilon_0\varepsilon_t}{\pi}\right) \sum_{n=1}^{\infty} \frac{1}{2n-1} J_0^2 \left(\frac{(2n-1)\pi s}{2(s+w)}\right)
## Capacitance for very Thin Interdigitated Fingers

<table>
<thead>
<tr>
<th>Equation</th>
<th>Capacitance, C = 2.26E-12 F</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C = \sum_{n=1}^{\infty} \frac{1}{2n-1} \log \left( 1 + \frac{(2n-1)\pi r}{2(s+w)} \right)$</td>
<td>Number of Fingers, N = 120</td>
</tr>
<tr>
<td>relative dielectric constant, $\varepsilon_r$ = 4.9</td>
<td>Length of finger overlap, $L$ = 440 $\mu$m</td>
</tr>
<tr>
<td>width of fingers, $w$ = 3 $\mu$m</td>
<td>space between fingers, $s$ = 3 $\mu$m</td>
</tr>
</tbody>
</table>

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Poly Heater on top of Diodes

Integrated series well resistor.
DIODES AND HEATER TEST RESULTS

Heater at 10 volts

\[ T = 25 + 0.04V/(2.2\text{mV/°C}) \]
\[ = 43.2 \, ^\circ\text{C} \]

Heater at 20 volts

\[ T = 25 + 0.11V/(2.2\text{mV/°C}) \]
\[ = 75 \, ^\circ\text{C} \]
RESISTORS

N+ Poly
(missing contact cuts)

6 different Resistor Designs

Nwell in P substrate

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RESISTORS

NWell
R = 1/SLOPE
= 1/0.025m
= 40,000 ohm
Rhos = 40K/39
=1026 ohm/sq

Poly
R = 1/SLOPE
= 1/0.681m
= 1468 ohm
Rhos = 1468/39
=37.6 ohm/sq
RESISTORS

R=12K ohms
Theoretical R = Rhos L/W
= 45 (12*390)/9 = 23K

R=37.1K ohms
Theoretical R = Rhos L/W
= 45 (12*390)/6 = 35K

R= 139K ohms
Theoretical R = Rhos L/W
= 45 (12*390)/3 = 70K
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RESISTORS

390/10um 390/30um L/W

R = 1/slope
Rhos = R W/L

Poly
R=1468
Rhos=37.6

nWell
R=44K
Rhos=1.13K

Pwell
R=4160
Rhos=320

P+ in nWell
R=1.78K
Rhos=45.7

n+ in pWell
R=1.46K
Rhos=37.4

P+ in nWell
R=582
Rhos=44.8

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PHOTOVOLTAIC DEVICES

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8 cell battery  dual cells  single cell

~350µm  by  ~350µm

P+ in Nwell
SINGLE AND DUAL PHOTO CELL

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Isc = 1.088 uA
or 6 A/m²

Isc = 0.585 uA
or 3.25 A/m²
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**8-CELL PHOTO BATTERY**

---

**Design Errors**

N- Wells too close
N+ and P+ not correct

---

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BIG PHOTO VOLTAIC CELL

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LARGE 5mm X 5mm PHOTODIODE

Isc = 0.15mA (short circuit current) or 9.09 A/m²
Primitive Cells
INVERTER, NAND2,3,4, NOR2,3,4, NULL

Basic Cells
XOR, MUX, DEMUX, ENCODER, DECODER
FULL ADDER, FLIP FLOPS

Macro Cells
BINARY COUNTER
SRAM
PRIMITIVE CELLS WITH PADS

INV/NOR4  NOR3/NAND2  NOR2/NAND3  INV/NAND4

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**CMOS INVERTER**

Vin → Vout

Vin

\[ +V \]

\[ I_{dd} \]

PMOS

Vout

NMOS

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>VIN</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

W = 40 \(\mu m\)
L\text{drawn} = 2.5\(\mu m\)
L\text{poly} = 1.0\(\mu m\)
L_{eff} = 0.35 \(\mu m\)

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INVERTER TEST RESULTS

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PRIMITIVE CELLS

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PRIMITIVE CELLS

NAND2

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NOR2

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NOR3
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NOR4

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**BASIC DIGITAL CELLS WITH PADS**

- Multiplexer
- XOR
- Full Adder
- Encoder
- Decoder
- Demux

Edge Triggered DFF

JK FF
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4 TO 1 MULTIPLEXER

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4 TO 1 MULTIPLEXER
BASIC CELL XOR

Input A

Port in → A' → A'B

Input B

Port in → B → B' → AB'

XOR = A'B + AB'

Port out → XOR

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XOR

NOT CORRECT

Output Inverted
FULL ADDER

MISSING VIA
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DECODER

Correct
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ENCODER

Digital Encoder

Coded Output Lines

512 inputs can be coded into 9 lines which is a more dramatic benefit

A B C D | Q0 Q1
1 0 0 0 | 0 0
0 1 0 0 | 0 1
0 0 1 0 | 1 0
0 0 0 1 | 1 1

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EDGE TRIGGERED D TYPE FLIP FLOP

Positive Edge Triggered D FF

Inputs | Outputs
--- | ---
D | C | Q | Q
0 | 1 | 0 | 1
1 | 1 | 1 | 0
X | 0 | Q | Q
X | 1 | Q | Q
D FLIP FLOP WITH SET AND RESET
JK FLIP FLOP

Positive Edge Triggered JK FF

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>J</td>
<td>Q</td>
</tr>
<tr>
<td>K</td>
<td>C</td>
</tr>
<tr>
<td>C</td>
<td>Q</td>
</tr>
<tr>
<td>Q̅</td>
<td>0</td>
</tr>
<tr>
<td>J</td>
<td>1</td>
</tr>
</tbody>
</table>

CLK

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**T-TYPE FLIP-FLOP**

Toggel Flip Flop

Q: Toggles High and Low with Each Input

<table>
<thead>
<tr>
<th>T</th>
<th>Qn-1</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

T Flip Flop is a JK FF With J and K connected together and labeled T
BINARY COUNTER USING T TYPE FLIP FLOPS

State Table for Binary Counter

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>F-F Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A  B  C</td>
<td>A  B  C</td>
<td>T_A  T_B  T_C</td>
</tr>
<tr>
<td>0  0  0</td>
<td>0  0  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>0  0  1</td>
<td>0  1  0</td>
<td>0  1  1</td>
</tr>
<tr>
<td>0  1  0</td>
<td>0  1  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>0  1  1</td>
<td>1  0  0</td>
<td>1  1  1</td>
</tr>
<tr>
<td>1  0  0</td>
<td>1  0  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>1  0  1</td>
<td>1  1  0</td>
<td>0  1  1</td>
</tr>
<tr>
<td>1  1  0</td>
<td>1  1  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>1  1  1</td>
<td>0  0  0</td>
<td>1  1  1</td>
</tr>
</tbody>
</table>

Input Pulses

Toggel Flip Flop

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3-BIT BINARY COUNTER WITH D FLIP FLOPS

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8-BIT BINARY COUNTER

COUNT PULSES

COUNT ENABLE

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8-BIT BINARY COUNTER
8-BIT BINARY COUNTER WITH PADS
MACROCELLS

3-Bit Binary Counter / Shifter
8-Bit Binary Counter / Shifter
SRAM
Microcontroller
Etc.
ADDITIONAL CIRCUITRY TO RESET, SHIFT, COUNT
3-BIT BINARY COUNTER/SHIFT REGISTER

Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit
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SRAM

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Operational Amplifier
Inverter with Hysteresis
RC Oscillator
Two Phase Clock
Analog Switches
Voltage Doubler, Tripler
Analog Multiplexer
Comparator with Hysteresis
A-to-D
D-to-A
OTA, Biquad Filter, Elliptic Filter
Programmable Binary Weighted Resistors
SPICE PARAMETERS FOR SUB-CMOS PROCESS

*This file is called: RIT_MICROE_MODELS.TXT
*
*1-15-2007 FROM DR. FULLER’S SPREADSHEET WITH VT0=0.75
_sampler_49 NMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8 NSS=3E11
+XWREF=2.0E-7 XLREF=2.95E-7 VTH0=0.75 U0= 950 WINT=2.0E-7 LINT=1.84E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGS0=3.4E-10 CGD0=3.4E-10 CGB0=5.75E-10)
*
*1-17-2007 FROM DR. FULLER’S SPREADSHEET WITH VT0=-0.75
_sampler_49 PMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8 NSS=3E11 PCLM=5
+XWREF= 2.0E-7 XLREF=3.61E-7 VTH0=-0.75 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 NGATE=5E20
+CGS0=4.5E-10 CGD0=4.5E-10 CGB0=5.75E-10)
*
OPERATIONAL AMPLIFIER

Version 1

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VERSION 1 OPERATIONAL AMPLIFIER

p-well CMOS

dimensions
L/W
(µm/µm)

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**R/C 2/2 OpAmp**

**CMOS INVERTER**

**Conditions:**
- Con. SMU1
  - Val: 5.0000 V
- Con. SMU2
  - Val: 0.0000 A
- Con. SMU4
  - Val: -5.0000 V
- Svs: SMU3
  - Start: -1.0000 V
  - Step: 1.0000 V
  - Step: 2.0000m V
  - Pts: 1001

<table>
<thead>
<tr>
<th>Fit #1</th>
<th>Fit #2</th>
<th>Cursors: X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type:</td>
<td>Cursor</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Slop:</td>
<td>4.9900</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yint:</td>
<td>-24.5590</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Xint:</td>
<td>5.0223</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Op Amp**

- Gain: **-4.89k**
- Offset: **0** m Volts
- GBW: **Hz**

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**OPAMP 1**

All had missing metal one due to over etch. Metal lines at 3µm.

Redesign with bigger metal lines.
OpAmp: 1 R/C 2/2

<table>
<thead>
<tr>
<th></th>
<th>Op Amp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>-2.4k</td>
</tr>
<tr>
<td>Offset</td>
<td>47 m Volts</td>
</tr>
<tr>
<td>GBW</td>
<td>Hz</td>
</tr>
</tbody>
</table>
### OPAMP 2

#### CMOS INVERTER

<table>
<thead>
<tr>
<th>Conditions:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Con: SMU1</td>
<td></td>
</tr>
<tr>
<td>Val: 5.0000 V</td>
<td></td>
</tr>
<tr>
<td>Con: SMU2</td>
<td></td>
</tr>
<tr>
<td>Val: 0.0000 A</td>
<td></td>
</tr>
<tr>
<td>Con: SMU4</td>
<td></td>
</tr>
<tr>
<td>Val: -6.0000 V</td>
<td></td>
</tr>
<tr>
<td>Swp: SMU3</td>
<td></td>
</tr>
<tr>
<td>Start: -5.0000 V</td>
<td></td>
</tr>
<tr>
<td>Stop: 5.0000 V</td>
<td></td>
</tr>
<tr>
<td>Step: 0.0100 V</td>
<td></td>
</tr>
<tr>
<td>Pts: 1001</td>
<td></td>
</tr>
</tbody>
</table>

#### Op Amp Data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>-939</td>
</tr>
<tr>
<td>Offset</td>
<td>-1.6 Volts</td>
</tr>
<tr>
<td>GBW</td>
<td>Hz</td>
</tr>
</tbody>
</table>
TWO PHASE CLOCK

CLOCK

CLOCKBAR

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ t_1 \]

\[ t_2 \]

\[ t_3 \]

\[ R \]

\[ Q \]

\[ S \]
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TWO PHASE NON OVERLAPPING CLOCK

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TWO PHASE CLOCK

Circuit of previous page at 100Khz
NEW TWO PHASE CLOCK

- **CLOCK**: R, t_1, Q, Φ_1
- **CLOCKBAR**: S, t_2, Φ_2

Diagram showing a two-phase clock circuit with inverters and logic gates.
WINSPICE SIMULATION FOR VERSION TWO + BUFFERS

Next Design add buffers
ANALOG SWITCH

Vin

D

S

D

S

Vout

+V

0-5V Logic Control

+5

-V

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VOLTAGE DOUBLER / TRIPLER

Voltage Tripler

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**OPERATIONAL TRANSCONDUCTANCE AMPLIFIER**

**CMOS Realization**

![CMOS Amplifier Diagram]

Note: \( gm \) is set by \( I_{bias} \)

---

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SPICE ANALYSIS OF CIRCUIT ON PREVIOUS PAGE

Homework Assignment
**BIQUAD FILTER**

\[
V_{\text{out}} = \frac{(s^2C_1C_2V_c + sC_1g_{m4} V_b + g_{m2} g_{m5} V_a)/(s^2C_1C_2 + sC_1g_{m3}+g_{m2}g_{m1})}{s^2C_1C_2/g_m + sC_1/g_m + 1}
\]

This filter can be used as a low-pass, high-pass, bandpass, bandrejection and all pass filter. Depending on the C and gm values a Butterworth, Chebyshev, Elliptic or any other configuration can be achieved.

For example: let \(V_c=V_b=0\) and \(V_a=V_{\text{in}}\), also let all \(g_m\) be equal, then

\[
V_{\text{out}} = \frac{V_{\text{in}}}{(s^2C_1C_2/g_m g_m + sC_1/g_m + 1)}
\]

which is a second order low pass filter with corner frequency at

\[
\omega_c = \frac{g_m}{\sqrt{C_1C_2}} \quad \text{and} \quad Q = \sqrt{\frac{C_2}{C_1}}
\]
3 BIT ANALOG TO DIGITAL CONVERTER

Comparators

Segment Detector

Decoding Logic

Vin

8V  +V

3.5V

7V

6V

5V

4V

3V

2V

1V

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Page 114
3 BIT ANALOG TO DIGITAL CONVERTER
8 TO 1 ANALOG MUX
3 BIT D TO A

Vref

b1

b1

b2

b2

b3

b3

MSB

Vout

LSB

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Comparator With Hysteresis
Voltage Controlled Oscillator
Binary Weighted R-2R Current Source
EEPROM
Binary Weighted EEPROM Selected Current Source
CCD
CCD Shift Register
More…
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PROJECTS

Wireless Capacitive Sensor
Spectro Photometer
Hearing Aid
CCD Imager
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WIRELESS CAPACITIVE SENSOR PROJECT

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Page 121
Many of these circuits need Up/Down counters and shift registers. In the next few pages we will look at one type of counter and see how to modify it to also function as a shift register.
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SPECTROPHOTOMETER

7-Bit Analog Multiplexer

- D1
- D2
- D3
- D4
- D5
- D6
- D7
- D8

SWITCHES

A
A
B
B
C
C

128 PHOTODIODES

7-BIT COUNTER

Analog out

Sync pulse (at 0000000B)

Clock

Reset

Rochester Institute of Technology
Microelectronic Engineering

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HEARING AID PROJECT

- **PREAMPLIFIER**
- **AUTOMATIC GAIN CONTROL**
- **STATE VARIABLE**
- **VARIABLE HIGH PASS**
- **OUTPUT BUFFER**

**Not Done**

**Biquad Filters**
**EEPROM**
**MEMS Microphone**
**MEMS Speaker**
**Energy Harvesting**

- **MICROPHONE**
- **RECEIVER**

4th Order High Pass
- Pole Constant, Zero Varied
- Zero Constant, Pole Varied

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PACKAGING

Wire Bond Pads
SODIMM Connectors
(Zero Insertion Force)
Solder Bump
Pads ~0.22mm x 0.22mm
With ~ 0.030mm space
Wire is ~75µm diameter
Bond is ~150 µm diameter
**S.O.DIMM CONNECTOR**

144 CONTACT(S), FEMALE, RIGHT ANGLE SINGLE PART CARD EDGE CONN, SURFACE MOUNT, SOCKET

This product ships from a Jameco satellite warehouse, usually within 2 to 3 the next business day when received by 5:00PM EST. Please choose expedited processing at checkout if you prefer to have the other products on your order ship immediately. Separate shipping charges would then apply.

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<th>Jameco P/N</th>
<th>801588PS</th>
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<td>BOARD</td>
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<td>Terminal Pitch (mm)</td>
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**We temporarily have this product available at this lower price.** Supply runs of this quantity will be limited.

**View Tech Data Sheet**

**Download / Font Pack**
SOLDER BUMP TEST CHIP

1000µm center-to-center
225µm diameter circle

Under bump metal is Cr/Ni and is defined by a lift-off lithography.

The solder is printed using a 150µm photoresist and solder paste. (or 500µm solder ball is placed over circle)
RIT SOLDER BUMPS

~500µm
REFERENCES

9. MOSIS SCMOS at http://www.mosis.com
10. Texas Instruments, Data Sheet for inverter with hysteresis.
HOMEWORK

1. Calculate the expected values of the poly heaters over the diode temperature sensors on page 47.
2. For the PMOS transistor shown on page 29 determine Lambda, Idrive, gm max, and Vt. Use correct units as shown on page 25-27.
3. Why is the gate delay different for the two ring oscillators shown on page 33.
4. List the digital circuits that were shown to be working correctly in this document.
5. Write a 150 word abstract for the John Galt Chip and the test results shown in this document.