Data Conversion Circuits
A-to-D and D-to-A

Dr. Lynn Fuller

Webpage: http://people.rit.edu/lfsee
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5004

Email: Lynn.Fuller@rit.edu
Department webpage:
https://www.rit.edu/engineering/electrical-and-microelectronic-engineering

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INTRODUCTION

Analog electronic circuits are different from digital circuits in that the signals are expected to have any value rather than two discrete values. **Primitive** analog components include the diode, mosfet, BJT, resistor, capacitor, etc. Analog circuit **building blocks** include single stage amplifiers, differential amplifiers, constant current sources, voltage references, etc. **Basic** analog electronic circuits include the operational amplifier, inverting amplifier, non-inverting amplifier, integrator, bistable multivibrator, peak detector, comparator, RC oscillator, etc. **Mixed-mode** analog integrated circuits include D-to-A, A-to-D, etc.

This document will introduce some **mixed-mode** analog/digital electronic circuits.
OUTLINE

Analog Multiplexer
D to A
A to D
Binary Counter A to D
Flip Flops
Shift Registers/Counters
Design Examples
Blue Tooth
References
Homework
An analog multiplexer is basically a bunch of transistor switches that can connect one of the inputs to the output, \( V_{out} \) depending on which switches are closed. This schematic is an analog multiplexer with three binary inputs. The truth table shows which input will be connected to \( V_{out} \). For example when the binary input \((b1, b2, b3)\) are all zero then \( V1 \) is connected to \( V_{out} \). No other path is connected. If the input is \((111)\) then \( V8 \) is connected to \( V_{out} \).

<table>
<thead>
<tr>
<th>MSB b3 b2 b1</th>
<th>Vout</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>V1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>V2</td>
</tr>
<tr>
<td>0 1 0</td>
<td>V3</td>
</tr>
<tr>
<td>0 1 1</td>
<td>V4</td>
</tr>
<tr>
<td>1 0 0</td>
<td>V5</td>
</tr>
<tr>
<td>1 0 1</td>
<td>V6</td>
</tr>
<tr>
<td>1 1 0</td>
<td>V7</td>
</tr>
<tr>
<td>1 1 1</td>
<td>V8</td>
</tr>
</tbody>
</table>

Each switch is a PMOS transistor.
This SPICE shows the switches for a two bit analog multiplexer. The gates of the switches are connected to digital level signals that might be too low to insure that the switches are on enough to drive the load. The level shifting circuit between the digital logic input and the gates of the multiplexer switches increase the voltages to +5 and -5 in this circuit.
This is a layout of the switch part of the analog multiplexer. It can be very compact. The digital logic and level shifting is not shown.
This shows the use of an analog multiplexer to read the current generated by a 128 photodiode array. 128 x 7 transistors for the switch matrix, a 7 bit counter logic plus some other circuitry. In this example the analog output is a current that is converted to a voltage using an op amp current to voltage converter.
A digital to analog converter (D to A) can be realized by using an analog multiplexer where the analog inputs are fixed at specific voltages (some fraction of a reference voltage). A 3-bit D-to-A can output 8 different voltage levels… 0 to 7/8 times the reference voltage.
To make the math easier let's pick a reference voltage of 8 volts and use 8 identical value resistors in series. The 8 volt reference will create one volt across each of the eight resistors. The switches connect from 0 volts up to $\frac{7}{8} \times V_{\text{ref}} = 7$ volts.
This is another way to create a digital to analog converter. The op amp will convert current to voltage. The current is \( I = i_1 + i_2 + i_3 \). That current must flow through the feedback resistor and ohms law give a voltage drop of \( I \) times \( R \). The left side of the feedback resistor is at zero volts (virtual ground). Thus the output voltage is negative \( I \) times \( R \). If the resistors in the switch matrix are binary weighted such that the first is \( R \), second is \( 2R \), third is \( 4 \) times \( R \), fourth is \( 8 \) times \( R \), and so on then the currents through those resistors will also be binary weighted. The largest current through \( R \) and decreasing from there. Making large value resistors on a chip takes up a lot of space.

With the switches as shown \( V_o = \frac{-V_{\text{ref}} R/2}{4R} = -V_{\text{ref}}/8 \)

What is \( V_o \) for a 101 digital input?
How is this architecture extended to more bits?
This type of architecture does not require increasing size resistors to realize binary weighted currents for each switch going into the op amp.
VLSI (Very Large Scale Integration) circuit design course are taught by EE, MicroE, and CE departments. Different design projects are assigned each year. This is an example of four student designs for a Digital to Analog converter for a VLSI course in CE. These CMOS integrated circuits were made by students in the MicroE department in a subsequent school term.
The data conversion examples in the previous pages were all related to D-to-A (or DAC) converters. The reason we looked at those first is because we want to use a DAC to make an Analog to Digital Converter (A-to-D). Shown above is an architecture for an A-to-D converter. A digital counter made with several flip-flops has a clock input and a count enable input. The comparator will be either high or low. Since the Analog input to be converted is connected to the non-inverting input the initial count enable value will be high and the counter will count up. The binary count from the flip-flops becomes the input to the Digital to Analog converter (DAC) and the output of the DAC is compared to the Analog Vin. When the DAC Vo equals the Analog Vin the counter stops counting. The conversion is complete and the digital value is available from the counter and can be displayed or used in other ways in the digital system. All of this can be done are at speeds determined by the clock frequency. For high bit count converters this can take many clock cycles and is not the fastest type of converter.
This is a different type of A-to-D converter. It is somewhat simpler in that it has less components. Conversion begins when the switch S1 is connected to the analog input and S2 is opened. The first op amp is an integrator. The current in R is \( i = -\frac{V_{in}}{R} \) and that current flows from right to left in the capacitor which charges up, \( V_x \) is \( \frac{1}{C} \) integral of \( I \) dt. At some fixed time later \( T_1 \) the switch S1 is connected to \( V_{ref} \) and the current flows in the opposite direction, now left to right in the capacitor \( C \). At \( T_1 \) the counter starts counting. The capacitor discharges at a rate determined by \( V_{ref} \) and when it reaches zero the comparator switches the output to low and the counter stops counting. The value in the counter is the digital output.
The flash is a fast architecture for doing A-to-D conversion. For high bit counts this type of converter will have a very large number of transistors, comparators, resistors, inverters, and logic gates. However today we can put millions (even billions) of transistors on a single chip.

The analog voltage to be converted is compared to discreet voltages generated from a reference voltage and a number of identical resistors in series. If the analog voltage is higher than the voltage from the resistors the comparator output is high, otherwise it is low. The inverter and AND gate make a segment detector where only one output is high and all the other outputs are low. The binary signal is generated in the decoding logic. The example shown here is for a 3.5 volt analog input.
This layout is from a flash A-to-D design for a 3-bit converter. The design was based on macrocells where the components in the white boxes were designed first and they were used in the system design. The resistors are not shown but everything else is shown.
Digikey offers over 15,000 Analog to Digital converters. Input single sided or differential, output serial or parallel, Voltage levels for analog input and digital output, various package types and prices from $0.45 each to $4500.00 each.
More selection parameters
REFERENCES

1. Design an R-2R 3-Bit D-to-A converter and show it works using SPICE.

2. Browse the Digikey on line selection guide and find a flash A to D converter. How fast is it?