EEE 482 Electronics II Laboratory

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OUTLINE

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INTRODUCTION

This laboratory course will provide a continuation of electronic circuit design that was the topic of EEEE 381 Electronics I.

About half of the course will cover traditional topics on bipolar analog integrated circuits. The second half will cover topics in digital electronics.

This course will enhance the students understanding of how SPICE parameters are linked to the manufacturing process and how to extract these parameters so they can be used by circuit designers.

This course will teach the student how to trouble shoot complex circuits, an important skill for engineers.
## INSTRUCTOR INFORMATION

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EEE 482 Electronics II Laboratory

Prerequisites: EEEE 360 (Semiconductor Device Physics) or Equivalent and EEEE 381 (Electronics I)

Course Goals: This is the second course in a two course sequence in electronic circuit design. The course will cover BJT and MOS analog and digital electronic circuit design.

Format: The lab meets one time per week except for the first week. Lab documents are posted on Dr. Fuller’s webpage.

Laboratory: 8:00am to 10:50am Monday GLE-3280  
2:30pm to 5:20pm Monday GLE-3280  
2:30pm to 5:20pm Wednesday GLE-3200

Laboratory Grade: Pre-lab 10% Individual  
Simulations 10% Individual  
Lab Performance 10% Group  
Each Tech Memo 10% Individual  

Note: any part missing will result in failing grade.
<table>
<thead>
<tr>
<th>Week</th>
<th>Topic</th>
<th>Document</th>
<th>References</th>
<th>Assignment</th>
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<tr>
<td>1.</td>
<td>Introduction, Schedule, Policies, Tech Memo Template (No lab meeting 1st week)</td>
<td><strong>IEEE 482 Lab Outline.pdf</strong></td>
<td><strong>Tech_Memo_Instructions.doc</strong> <strong>GradingComments.pdf</strong></td>
<td>Read These Documents</td>
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| 2.   | SPICE Review  
LT SPICE is very similar to OrcAD PSpice. It is free, has no limits on number of components and easy to use. Ideal for your personal computer. | **OrCAD PSpICE Intro.htm** **OrCAD PSpICE Intro.pdf** | **Intro to LTSPICE.htm**  
**RIT SPICE Models.txt**  
**Intro to LTSPICE.wvm**  
**Intro to LTSPICE.pdf** | Review LTSPICE  
Do SPICE Intro Examples |
| 5.   | Differential Amplifier with Resistive Load and Current Source Bias | **IEEE 482 Lab1 Rev2015 2.doc** **Diff Amp Lab.pdf** | | Tech Memo Due Next Week |
| 6.   | Multistage Amplifier Design | **IEEE 482 Lab2 Rev2015 2.doc** **DC Coupled Amp Lab.pdf** | | Tech Memo Due Next Week |
| 8.   | Review of Modeling MOSFETs in SPICE  
Work on your Prelab for NMOS Inverters (Long Prelab) | **Modeling MOSFETs in SPICE.pdf** **Modeling MOSFETs in SPICE.htm**  
**RIT Models For LTSPICE.txt**  
**CD4007 SPICE MODEL** | **SPICE MOSFET Models**  
**RIT Models For LTSPICE.txt**  
**CD4007 SPICE MODEL** | Review these documents |
| 10.  | CMOS Inverter and Combinatorial Logic | **IEEE 482 Lab5 Rev2015 1.doc** **CD4007 SPICE MODEL** **CMOS Inverter Lab.pdf** | | Tech Memo Due Next Week |
| 11.  | CMOS Sequential Logic | **IEEE 482 Lab6 Rev2015 1.doc** **Sequential Logic.pdf** | | Tech Memo Due Next Week |
| 12.  | Propagation Delay in CMOS Logic | **IEEE 482 Lab7 Rev2015 1.doc** **CMOS_Ring_Oscillator_Lab.pdf** | | Tech Memo Due Next Week |
| 13.  | MOS Based Memory | **IEEE 482 Lab8 Rev2015 1.doc** **SRAM** | | Tech Memo Due Next Week |
| 14.  | No Labs | | | |
ATTENDANCE

Attendance is mandatory. If you have a valid reason for missing lab, inform your TA/Instructor **before** the day of the lab. Laboratories will be made up by appointment only. Possibly during one of the other lab meeting times or when no lab is scheduled. **It is your responsibility to inform the TA/Instructor in advance and to schedule a time slot during which to make up the experiment.**
LABORATORY REPORTS

Use the Tech Memo Format. Submit the Tech Memo via MyCourses dropbox. The reports are due one week after the lab work is completed late reports will be graded but may have the grade lowered.

Grading: Each Lab is 40 points. Any part missing will result in a failing grade for that lab.

Pre-Lab Hand Calculations 10 points
Pre-Lab SPICE 10 points
Build and Data Collection 10 points
Tech Memo
  Abstract 5 points
  Theory or Design 1 points
  Results 2 points
  Discussion 2 points
LATE POLICY

Reports are generally due at the beginning of class when the lab next meets. For example, if your lab is on Monday, your lab report is due at the beginning of lab on the next Monday that the lab meets.

The maximum late penalty for a given report is 50%. The maximum grade for labs handed in after seven days is 50%.

No reports will be accepted after 5 PM on Friday the last day of classes.
PRE LAB

The pre-lab for each experiment MUST be completed BEFORE coming to the lab. If you do not understand a part of the pre-lab, then it is your responsibility to get help before the lab. Pre-lab theoretical calculations must be done individually and be presented neatly at the beginning of lab on a separate sheet of paper and included in the Tech Memo as an appendix. The pre-lab helps you understand how to perform the lab, what is being done, and how to interpret your results. It is to your benefit to have the pre-lab done in advance. You will be penalized if your pre-lab is not completed when the TA/Instructor comes around to check it off.

SPICE Simulations must be presented electronically. The schematic and resulting waveforms, node voltages and branch currents available to show and discuss with the instructor.
Simulation is expected to be performed on OrCAD Capture CIS. Students may use the PCs in the CEDA lab or any of the other labs they may have access to. Capture CIS is installed on all PCs on the EE (3rd) floor. You can obtain an Orcad Lite Demo CD for free by visiting [http://www.orcad.com/](http://www.orcad.com/) and clicking on the download link. The Demo CD will be mailed to you after filling out the user profile. You can also download the student version from the website as well. It’s a zipped file that is about 28MB in size.

It should be noted that simulation is meant to be used for confirmation of hand design before the construction of the circuit in the laboratory. It is poor engineering practice to use the simulation for designing circuits by a trial-and-error method, as this reinforces a lack of understanding of the circuit design process.
The pre-lab and simulation portions of each experiment should be done individually. Students can work in groups of up to two people for the hardware portion of each experiment. At the time of hardware check-off, both students in the group must be present and present their circuit for verification. Each student must turn in his/her own, original report. Reports are not to be completed in groups.
LABORATORY SUPPLIES

Prototype board
Breadboard supplies – wires, pliers, wire stripper, tape, scissors
RECOMMENDATIONS

Pre-Lab

Hand calculations can be included as an appendix in the lab report. (as a scan or picture)

SPICE Simulations:
Schematic should show DC voltages and currents, transistor L and W and other properties.
The transistor model used for the simulation needs to be justified and described in the report.
Plots should have white background, the graph lines should be thick, text should be big enough to read.

Hardware Build:
Oscilloscope data should be collected with two scope probes.
Abstract (MOST IMPORTANT PART OF REPORT)
The abstract should be 3 or 4 sentences that describe the work and give the most important results. If someone reads the abstract they should not need to read the rest of the lab unless more detail is desired.

Theory and Design
Theory, Calculations, SPICE

Results
All the data collected in lab.

Discussion
You may wish to use the following textbooks as references. Lab documents are will be provided on Dr. Fuller’s webpage.


5. PSPICE Users Guide.