A Student Run Integrated Circuit Factory at Rochester Institute of Technology

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Microelectronic Engineering

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OUTLINE

§ Student Run Factory and Facilities
§ CIM System
§ RIT’s Sub Micron CMOS Process
§ MESA Factory Definition, Processes, Products
§ Factory Operation, Protocol and Measures
§ Six Sigma Processing
§ Statistical Process Control
§ Results
§ Future Work
§ Conclusion
§ Homework
STUDENT RUN FACTORY

- Masters Level and Undergraduate Level Students in Microelectronics Manufacturing Courses are the Operators
- Submicron CMOS Processes, Advanced CMOS (deep Submicron)
- Customers are Faculty and Students at RIT
- Products Include Extensive Test Chip, Analog Circuits (Op Amps, OTA’s, Filters) & Digital Circuits.
- In 2010 the Factory Processed 43 Lots (3 wafers each), 129 wafers were started, 104 were completed (25 were scraped)
GOALS

§ Provide Students with Training in all Unit Processes
§ Provide a Laboratory for Teaching Semiconductor Manufacturing Topics such as:
  § WIP tracking
  § CIM
  § Cycle Time Management
  § Real Time SPC
  § Six Sigma and TQM Methodologies
§ Provide a CMOS Foundry Service
BENEFITS

§ Documentation for tools must be very good including
  § mini operation manuals
  § log sheets and maintenance Logs
§ A WIP tracking system must be developed
§ Lot History and Data is reliably collected
§ Baseline manufacturing process is maintained
LABORATORY FACILITY

§ 1986
§ 15,000 sq. ft.
§ Class 1000, 100, 10
§ Complete CIM System
§ E-beam Maskmaking
§ Mentor Graphics Design Tools
§ Surface Analysis Lab
§ 100 and 150 mm Wafers

§ Complete Equipment Set
§ Ion Implanter
§ LPCVD Poly, Nitride and Oxide
§ PECVD TEOS Oxide, Nitride
§ Oxide/Diffusion Furnaces
§ Reactive Ion Etch
§ 5X i-line Wafer Stepper
§ Coat and Develop Track Systems
§ Plasma Asher
§ Sputtering System
§ Measurement Tools
§ Rapid Thermal Processor
§ Chemical Mechanical Polishing
CIM SYSTEM

§ AS/400
§ Many PC Workstations
§ Ethernet LAN
§ Quality Analyst Software
§ MESA Software (Manufacturing Execution System Application)
  § Work-in-process Tracking
  § Transaction Processing
  § Production Costs
  § Scheduling
  § Statistical Process Control
  § Resource Management
§ On-Line Reporting
  Lot Status
  Transaction History
  Data Collection
  Specifications and Instructions
CIM SYSTEM HARDWARE

RIT Campus Network

VAXC
VT Terminal
VT Terminal
LAT
LAT
ETHERNET
RS-232
ETHERNET
DELNI

RIT MicroE CIM System

AS-400
PC’s Terminal
PC’s Terminal
PC’s Terminal
PC’s Terminal
CIM SYSTEM - PC WORKSTATION
USER INTERFACE

Select one of the following:
1. Start
2. Move-in
3. Move-out
4. Ship
5. Lot Status of All Lots
6. What’s next for a Lot
7. Mask ID & Stepper Job Information
8. Process Master Inquiry
9. Lot History/Move Summary
10. Query Processing Menu
11. Process Master Maintenance
90. Sign Off

Selection or Command

--->

F3 = Exit  F4 = Prompt  F5 = Refresh  F9 = Retrieve  F12 = Cancel
RIT is supporting two different CMOS process technologies. The older p-well CMOS and SMFL-CMOS have been phased out. The SUB-CMOS process is used for standard 3 Volt Digital and Analog integrated circuits. This is the technology of choice for teaching circuit design and fabricating CMOS circuits at RIT. The ADV-CMOS process is intended to introduce our students to process technology that is close to industry state-of-the-art. This process is used to build test structures and develop new technologies at RIT.

RIT p-well CMOS  \( \lambda = 4 \ \mu m \)  \( L_{min} = 8 \ \mu m \)
RIT SMFL-CMOS  \( \lambda = 1 \ \mu m \)  \( L_{min} = 2 \ \mu m \)
RIT Sub\( \mu \)-CMOS  \( \lambda = 0.5 \ \mu m \)  \( L_{min} = 1.0 \ \mu m \)
RIT Advanced-CMOS  \( \lambda = 0.25 \ \mu m \)  \( L_{min} = 0.5 \ \mu m \)
RIT Subµ CMOS

150 mm wafers, p-type
N_{sub} = 1E15 cm^{-3}
N_{n-well} = 3E16 cm^{-3}
X_{j} = 2.5 \mu m
N_{p-well} = 1E16 cm^{-3}
X_{j} = 3.0 \mu m
LOCOS
Field Ox = 6000 \AA
X_{ox} = 150 \AA
L_{min} = 1.0 \mu m
LDD/Side Wall Spacers
2 Layers Aluminum

3 Volt Technology
VT’s = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)
RIT SUBμ CMOS

NMOSFET

- N+ Poly
- N+ D/S
- Channel Stop
- LDD

PMOSFET

- 0.75 μm Aluminum
- 6000 Å Field Oxide
- LDD
- P+ D/S
- n+ well contact

P-type Substrate 10 ohm-cm
SUB-CMOS Versions 150

1. CL01
2. OX05 --- pad oxide, Tube 4
3. CV02 - 1500 Å
4. PH03 –1- n well
5. ET29
6. IM01 – n-well
7. ET07
8. CL01
9. OX04 – well oxide, Tube 1
10. ET19
11. IM01 – p-well
12. OX06 – well drive, Tube 1
13. ET06
14. CL01
15. OX05 – pad oxide, Tube 4
16. CV02 - 1500 Å
17. PH03 –2- Active
18. ET29
19. ET07
20. PH03 - -Pwell Stop

21. IM01- stop
22. ET07
23. CL01
24. OX04 – field, Tube 1
25. ET19
26. ET06
27. OX04 – Kooi, Tube 1
28. IM01 – Blanket Vt
29. PH03 – 4-PMOS Vt Adjust
30. IM01 - Vt
31. ET07
32. ET06
33. CL01
34. OX06 – gate, Tube 4
35. CV01 – Poly 5000A
36. IM01 - dope poly
37. OX08 – Anneal, Tube 3
38. DE01
39. PH03-5-poly
40. ET08
41. ET07
42. PH03 – 6 - n-LDD
43. IM01
44. ET07
45. PH03 – 7 - p-LDD
46. IM01
47. ET07
48. CL01
49. CV03 –TEOS, 5000Å
50. ET10
51. PH03 – 8 - N+D/S
52. IM01 – N+D/S
53. ET07
54. PH03 – 9 P+ D/S
55. IM01 – P+ D/S
56. ET07
57. CL01 Special - No HF Dip
58. OX08 – DS Anneal, Tube 2,3
59. CV03 – TEOS, 4000Å
60. PH03 – 10 CC
61. ET26
62. ET07
63. CL01 Special - Two HF Dips
64. ME01
65. PH03 -11- metal
66. ET15 – plasma Etch Al
67. ET07
68. SI01
69. CV03 – TEOS- 4000Å
70. PH03 – VIA
71. ET26
72. ET07
73. ME01
74. PH03- M2
75. ET15
76. ET07
77. SEM I
78. TE01
79. TE02
80. TE03
81. TE04
NA = 0.48 to 0.60 variable
σ = 0.35 to 0.85 variable

With Variable Kohler, or
Variable Annular illumination

Resolution = K1 \( \frac{\lambda}{NA} \)
\[\approx 0.35 \mu m \]
for NA=0.6, \( \sigma = 0.85 \)

Depth of Focus = \( k_2 \frac{\lambda}{(NA)^2} \)
\[\geq 1.0 \mu m \text{ for } NA = 0.6 \]

ASML 5500/200

i-Line Stepper \( \lambda = 365 \text{ nm} \)
22 x 27 mm Field Size
ASML MASK

Chrome Side
Mirrored 90°
Chip Bottom at Bottom

Non Chrome Side
As loaded into Reticle Pod,
Chrome Down, Reticle Pre-
Alignment Stars Sticking out
of Pod
RIT SUB-CMOS PROCESS

NMOSFET
- N+ Poly
- P+ D/S
- LDD
- Channel Stop
- 6000 Å Field Oxide
- 0.75 μm Aluminum

PMOSFET
- N+ D/S
- LDD P+ D/S
- n+ well contact

P-type Substrate 10 ohm-cm
- N-WELL
- P+ D/S
- n+ well contact

N+ Well Contact

LVL 1 – n-WELL
LVL 2 – ACTIVE
LVL 3 – STOP
LVL 4 – PMOS VT
LVL 5 – POLY
LVL 6 – P-LDD
LVL 7 – N-LDD
LVL 8 – P+ D/S
LVL 9 – N+ D/S
LVL 10 – CC
LVL 11 – METAL

11 PHOTO LEVELS
RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm⁻³ or 10 ohm-cm, n or p
Nn-well = 1E17 cm⁻³
Xj = 2.5 µm
Np-well = 1E17 cm⁻³
Xj = 2.5 µm
Shallow Trench Isolation
Field Ox = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin= 0.5 µm
LDD/Nitride Side Wall Spacers
TiSi2 Silicide
Tungsten Plugs, CMP, 2 Layers Aluminum
ADV-CMOS Versions 150, Two level Metal

1. OX05--- pad oxide 500 Å, Tube 4
2. CV02- 1500 Å Si₃N₄ Deposition
3. PH03 – level 1- STI
4. ET29 - etch Nitride
5. ET07 – ash
6. CL01 – RCA clean
7. OX04 – First Oxide Tube 1
8. ET06 – Etch Oxide
9. OX04 – 2nd Oxide Tube 1
10. PH03 – level 2 N-Well
11. IM01 – 3E13, P₃¹, 170 KeV
12. ET07 – ash
13. PH03 – level 3 – p-well
14. IM01 – 8E13, B¹¹, 80 KeV
15. ET07 – ash
16. ET19 – Hot Phos
17. OX06 – Well Drive, Tube 1
18. PH03 – NMOS Vt
19. IM01 – 3E12, B¹¹, 30KeV
20. ET07 - ash
21. PH03 – level 5 – PMOS Vₜ adjust
22. IM01 – 1.75E12, B¹¹, 60 KeV
23. ET07 – ash
24. ET06 – etch 500 Å pad oxide
25. CL01 – pre-gate oxide RCA clean
26. ET06 – etch native oxide
27. OX06 – 100 Å gate oxide, Tube 4
28. CV01 – poly deposition, 4000 Å
29. PH03 – level 6 – poly gate
30. ET08 – poly gate plasma etch
31. ET07 – ash
32. CL01 – RCA clean
33. OX05 – poly re-ox, 500 Å, Tube 4
34. PH03 – level 7 – p-LDD
35. IM01 – 4E13, B¹¹, 50 KeV
36. ET07 – ash
37. PH03 – level 8 – n-LDD
38. IM01 – 4E13, P₃¹, 60 KeV
39. ET07 – ash
40. CL01 – RCA clean
41. CV02 – nitride spacer dep
42. ET39 – sidewall spacer etch
43. PH03 – level 9 - N+D/S
44. IM01 – 4E15, P₃¹, 60 KeV
45. ET07 – ash
46. PH03 – level 10 - P+ D/S
47. IM01 – 4E15, B¹¹, 50 KeV
48. ET07 – ash
49. CL01 – RCA clean
50. OX08 – DS Anneal, Tube2,3
51. ET06 – Silicide pad ox etch
52. ME03 – HF dip & Ti Sputter
53. RT01 – RTP 1 min, 650C
54. ET11 – Unreacted Ti Etch
55. RT02 – RTP 1 min, 800C
56. CV03 – TEOS, P-5000
57. PH03 – level 11 - CC
58. ET06 – CC etch
59. ET07 – ash
60. CL01 – RCA clean
61. ME01 – Aluminum
62. PH03 – level 12-metal
63. ET15 – plasma Al Etch
64. ET07 – ash
65. CV03 – TEOS
66. PH03 – Via
67. ET26 Via Etch
68. ME01 Al Deposition
69. PH03 – Metal 2
70. ET07 - Ash
71. SI01 – sinter
72. SEM1
73. TE01
74. TE02
75. TE03
76. TE04

L = 0.5 μm
V_DD = 3.0 V
V_TN = 0.75 V
V_TP = - 0.75 V

(Revision 11-24-11)
KrF Excimer Laser Stepper
\( \lambda = 248 \text{ nm} \)
NA = 0.52, \( \sigma = 0.6 \)
Resolution = 0.7 \( \lambda / \text{NA} \approx 0.3 \mu \text{m} \)
20 x 20 mm Field Size
Depth of Focus = \( k_2 \lambda / (\text{NA})^2 \)
\( \approx 0.64 \mu \text{m} \)
6”x6” Masks
PRODUCTS

New John Galt Test Chip (Sub-CMOS and Adv-CMOS)

Older Obsolete Chips:
Mixed Analog/Digital Test Chip (Sub-CMOS Process)
Test Chip (Advanced CMOS Process)
John Galt Test Chip (Sub-CMOS Process)
4-Bit Microprocessor (Sub-CMOS Process)
Analog to Digital Converter (Sub-CMOS Process)
4-BIT MICROPROCESSOR
ANALOG TO DIGITAL CONVERTER

Output Register
Comp
DAC
Ref Buf
Successive Approximation Register
OPERATORS

Graduate and Undergraduate Students In Microelectronic Manufacturing Courses

Once or Twice Per Week for 3 or 4 hours

Goal is to do Operations that the Student has NOT Done Before And Learn how Each Process Works

Factory Operator Certification for:
- GCA and Canon Steppers Wafer Track
- RCA Clean
- Wet Oxide, Aluminum Etch Oxide Growth, Gate, Field Ox Diffusion, Sinter, Anneal
- LPCVD Poly, Nitride, Oxide Ion Implant
- Sputtering
- Metrology, 4pt Probe, Nanospec, CD, Overlay Test HP-4145, Probe Station
FACTORY MULTIDISCIPLINARY TEAMS

Every two weeks groups shift discipline (to the right). For example, the red group does Diffusion week 1&2, Red does Lithography week 3&4, Red does CVD/Plasma week 5&6, etc.

While in each discipline the students will
Process lots requiring steps in that discipline
Perform follow up Inspection and Metrology
Investigate and Update SPC data
Monitor non-device process metrics
Perform a “pass down” at the end of (2 weeks)
Track lots in and out of Mesa

Red Group
1. 2. 3.

Orange Group
1. 2. 3.

Yellow Group
1. 2. 3.

Green Group
1. 2. 3.

Blue Group
1. 2. 3.

Discipline

Process lots requiring steps in that discipline
Perform follow up Inspection and Metrology
Investigate and Update SPC data
Monitor non-device process metrics
Perform a “pass down” at the end of (2 weeks)
Track lots in and out of Mesa

Diffusion
Bruce Furnace
AG-RTP
Blue M Oven
Nanospec
Spectromap
CDE Resistivity Map

Lithography
Canon Stepper
SSI Track
CD Linewidth
Overlay
Branson Asher

PVD/Plasma Etch
CVC601
Drytech Quad
Lam490
Lam4600
Nanospec
Tencore P2

CVD/PECVD
ASM 6”LPCVD
P-5000
Nanospec
Spectromap
Varian 350D

Wet Etch/CMP
Al Wet Etch
BOE Etch
RCA Clean
Hot Phos Nitride Etch
BOE
Solvent Strip
CMP and CMP Clean
Nanospec
Surfscan
SEM
**OPERATOR FLOW CHART FOR FACTORY WORK**

START

Access MESA Lot Status

Find Queue Status
Step Number
Current Operation
Next Operation
Quantity

In Queue?  No → On Hold?  No → Mesa History Who Did Move-In

On Hold?  Yes → See Lab Instructor

Check Equipment Status

Apply Lot Selection Rules  Continue A

LOT SELECTION RULES

Do Photo first
Do Oldest Lot Next
Separate Lots Current Step
Match Skill Level
Use Equipment that is Up

Find Wafers

Preliminary Quality Check

On Hold?  Yes → Pass?

No → See Lab Instructor

Do Move-In Start Run Timer

Do Work Follow MESA Instructions Exactly

FINAL QUALITY CHECK

Count Wafers
Check Picture Log Book
Think
Refer to Previous Process Step
Check MESA Move-Out Comments

Pass?

Yes → Clean Up Return Wafers Return Masks

No → Stop Run Timer Move Out Record Data

END
## Lot Status Report

<table>
<thead>
<tr>
<th>Lot No</th>
<th>Product</th>
<th>Process / Version</th>
<th>Current Operation</th>
<th>Next Operation</th>
<th>Qty</th>
<th>Comments</th>
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<td>SUB-CMOS 150</td>
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Yellow and Green will do testing today
## OPERATOR PROCESS SIGNOFF SHEET

<table>
<thead>
<tr>
<th>Task</th>
<th>Date/Initials for Initial Training</th>
<th>Date/Initials Certified</th>
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<tr>
<td>CMP</td>
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<tr>
<td>CMP Clean</td>
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<td>SSI Track</td>
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<td>Branson Asher</td>
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<td>Wet Etch Oxide</td>
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<td>Wet Etch Nitride</td>
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<td>Al Etch</td>
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<td>CVD LTO</td>
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<td>Overlay Measurement</td>
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<td>Optical Pictures</td>
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STUDENT FACTORY PERFORMANCE MEASURES

- Wafer Moves Per Factory Day
- Wafer Moves x Operation
- Lot Starts/Ships/Scrap
- WIP
- Employee Moves Per School Quarter
- Lot Forward Advancement
- Cycle Time
Average is ~34 wafer moves/day

Average of 34 wafer moves per factory day. Compared to 50,000 to 100,000 wafer moves per day in industry.
### WAFER MOVES BY OPERATION

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<th># Wafers</th>
<th>Operation</th>
<th># Wafers</th>
<th>Operation</th>
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<td>RCA Clean</td>
<td>21</td>
<td>Starts</td>
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<td>CMP Clean</td>
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<td>Poly LPCVD</td>
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<td>18</td>
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<td>15</td>
<td>Scrap</td>
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</tbody>
</table>
LOT STARTS / SHIPS / SCRAP

For the Fall Quarter 2006
Lot Starts 7
Lot Ships 2
Lot Scraps 5
Work in Progress WIP (Lots) 12
Wafers Broken/Scraped 8
LOT FORWARD ADVANCEMENT

RIT FACTORY - LOT FORWARD ADVANCEMENT FOR WEEK
February 2, 1996 - February 8, 1996

LOT NUMBER

- F960109
- F951204
- F951025
- F950913
- F950724
- F950623

STEP NUMBER

0 10 20 30 40 50 60 70 80

# to go
#/week
Previous

Rochester Institute of Technology
Microelectronic Engineering
### CYCLE TIME & “X” FACTOR

<table>
<thead>
<tr>
<th>LOT #</th>
<th>FACTOR</th>
<th>STEP</th>
<th>CURRENT CALENDAR WEEKS</th>
<th>CURRENT FACTORY DAYS</th>
<th>FACTORY X</th>
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<tbody>
<tr>
<td>F950623</td>
<td>12.08</td>
<td>60</td>
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<td>102</td>
<td>8.50</td>
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<tr>
<td>F950724</td>
<td>13.89</td>
<td>45</td>
<td>25</td>
<td>90</td>
<td>10.00</td>
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<td>F950913</td>
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<td>21</td>
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<td>9.38</td>
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<td>F951025</td>
<td>10.94</td>
<td>32</td>
<td>14</td>
<td>54</td>
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<td>7.35</td>
<td>17</td>
<td>5</td>
<td>22</td>
<td>6.47</td>
</tr>
</tbody>
</table>

Theoretical is 25 lot moves/week
5 lot moves/factory day
SIX-SIGMA CONCEPTS

\[ \text{Cp} = \frac{\text{USL} - \text{LSL}}{6 \sigma} \]

\[ \text{K} = \frac{|\text{Tget} - \mu|}{(\text{USL} - \text{LSL})/2} \]

\[ \text{Cpk} = \text{Smallest of}: \left\{ \frac{\mu - \text{LSL}}{3 \sigma}; \frac{\text{USL} - \mu}{3 \sigma} \right\} \]

Reduce Variation
locate 6σ points within USL and LSL
Position Mean at Target
Goal of Cp=2.0, k=0, Cpk=2.0 to give less than 3.4 ppm
OXIDE GROWTH EXAMPLE

Change the furnace recipe so that RIT’s variable ramp down times do not affect the oxide thickness. Start soak time at 10 °C below soak temperature*

BEFORE:
- Push at 900 °C at 8 in/min in N2
- Ramp up 900 °C to 1100 °C in Dry O2
- Soak at 1100 °C in Dry O2 Time 1
- Ramp down from 1100 to 1000 °C in Dry O2
- Pull at 1000 °C at 8 in/min in N2

AFTER:
- Push at 900 °C at 8 in/min in N2
- Ramp up 900 °C to 1100 °C in Dry O2
- Soak at 1100 °C in Dry O2 Time 2*
- Ramp down from 1100 to 1000 °C in N2
- Pull at 1000 °C at 8 in/min in N2

*Start soak time at 10 °C below soak temperature.
IMPROVEMENT IN 5000 Å OXIDE GROWTH

Mar '94  Cpk = 0.38
Dec '94  Cpk = 0.77
# Measurement of Improvement in Cpk

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Dec 94</th>
<th>March 95</th>
<th>June 95</th>
<th>Sep 95</th>
<th>Dec 95</th>
<th>Mar 96</th>
<th>June 96</th>
<th>Sep 96</th>
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<tr>
<td></td>
<td>3 x Cpk</td>
<td>3 x Cpk</td>
<td>3 x Cpk</td>
<td>3 x Cpk</td>
<td>3 x Cpk</td>
<td>3 x Cpk</td>
<td>3 x Cpk</td>
<td>3 x Cpk</td>
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<tr>
<td>Masking Oxide Thick</td>
<td>1.14</td>
<td>2.31</td>
<td>2.31</td>
<td>3.75</td>
<td>3.25</td>
<td>3.26</td>
<td>2.53</td>
<td>2.25</td>
</tr>
<tr>
<td>Drive Oxide Thickness</td>
<td>2.51</td>
<td>2.20</td>
<td>2.17</td>
<td>3.31</td>
<td>3.15</td>
<td>3.20</td>
<td>3.25</td>
<td>3.41</td>
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<tr>
<td>Field Oxide Thickness</td>
<td>1.65</td>
<td>1.51</td>
<td>2.26</td>
<td>2.12</td>
<td>1.95</td>
<td>1.75</td>
<td>1.81</td>
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<tr>
<td>Gate Oxide Thickness</td>
<td>1.41</td>
<td>1.89</td>
<td>2.33</td>
<td>3.53</td>
<td>1.60</td>
<td>1.55</td>
<td>1.61</td>
<td>1.91</td>
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<tr>
<td>Kooi Oxide Thickness</td>
<td>0.07</td>
<td>0.29</td>
<td>0.45</td>
<td>1.60</td>
<td>1.10</td>
<td>0.42</td>
<td>0.43</td>
<td>0.42</td>
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<tr>
<td>Pad Oxide Thickness</td>
<td>0.58</td>
<td>1.07</td>
<td>2.07</td>
<td>2.17</td>
<td>1.65</td>
<td>1.84</td>
<td>1.87</td>
<td>2.02</td>
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<tr>
<td>Metal Thickness</td>
<td>0.31</td>
<td>0.99</td>
<td>0.59</td>
<td>1.10</td>
<td>1.15</td>
<td>1.10</td>
<td>1.16</td>
<td>1.20</td>
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<tr>
<td>N+ DS Rhos</td>
<td>0.23</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
<td>0.15</td>
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<tr>
<td>P+ DS Rhos</td>
<td>1.29</td>
<td>0.47</td>
<td>0.15</td>
<td>0.40</td>
<td>0.40</td>
<td>0.24</td>
<td>0.23</td>
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<td>Poly Thickness</td>
<td>0.92</td>
<td>2.25</td>
<td>2.00</td>
<td>1.36</td>
<td>1.18</td>
<td>1.29</td>
<td>1.29</td>
<td>1.26</td>
</tr>
<tr>
<td>Poly Rhos</td>
<td>1.53</td>
<td>1.53</td>
<td>1.53</td>
<td>2.41</td>
<td>2.41</td>
<td>1.08</td>
<td>1.08</td>
<td>1.03</td>
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<tr>
<td>Well Rhos</td>
<td>1.01</td>
<td>2.18</td>
<td>2.18</td>
<td>2.18</td>
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</tr>
</tbody>
</table>

Note: In December 95 we switched pad oxide from 1000 Å to 500 Å, Gate oxide from 700 Å to 500 Å, Kooi from dry to wet.

In June 96 we changed n+ dopant source to Emulsitone N250 to achieve lower sheet rho but we have not updated the new target, usl, isl.

Drain/source implants were doubled to lower sheet rho in January 96.
<table>
<thead>
<tr>
<th>SPC6SC_FO</th>
<th>Field Oxide Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPC6SC_GOX</td>
<td>Gate Oxide Thickness</td>
</tr>
<tr>
<td>SPC6SC_KOX</td>
<td>Kooi Oxide Thickness</td>
</tr>
<tr>
<td>SPC6SC_LTO</td>
<td>LTO/TEOX Oxide Thickness</td>
</tr>
<tr>
<td>SPC6SC_MTL</td>
<td>Metal Thickness</td>
</tr>
<tr>
<td>SPC6SC_N1</td>
<td>Nitride Thickness (1500Å)</td>
</tr>
<tr>
<td>SPC6SC_N2</td>
<td>Nitride Thickness (3500Å)</td>
</tr>
<tr>
<td>SPC6SC_PAD</td>
<td>Pad Oxide Thickness</td>
</tr>
<tr>
<td>SPC6SC_POL</td>
<td>Poly Thickness</td>
</tr>
<tr>
<td>SPC6SC_WO</td>
<td>Well Oxide Thickness</td>
</tr>
<tr>
<td>SPC6SCPROS</td>
<td>Poly Sheet Resistance</td>
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</tbody>
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NWA QUALITY ANALYST, SPC CHART

Pad Oxide
Target 500Å
USL 600Å
LSL 400Å
Mean 535Å
Std Dev 25Å
Cpk 0.8648
Cp 1.332
## PARTICULATE CONTAMINATION STUDY

<table>
<thead>
<tr>
<th>Tool</th>
<th>Before</th>
<th>After</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVC 601 Sputtering System</td>
<td>50</td>
<td>90</td>
<td>Clean</td>
</tr>
<tr>
<td>GCA 9001 Develop Line</td>
<td>70</td>
<td>200</td>
<td>Adds Particles</td>
</tr>
<tr>
<td>GCA 9001 Coat Line</td>
<td>100</td>
<td>200</td>
<td>Adds Particles</td>
</tr>
<tr>
<td>GCA Stepper</td>
<td>100</td>
<td>400</td>
<td>Adds Particles</td>
</tr>
<tr>
<td>Asher</td>
<td>50</td>
<td>200</td>
<td>Adds Particles</td>
</tr>
<tr>
<td>Varian 400 Ion Implanter</td>
<td>100</td>
<td>140</td>
<td>Clean</td>
</tr>
<tr>
<td>Furnace 12 Gate Oxide</td>
<td>40</td>
<td>50</td>
<td>Clean</td>
</tr>
<tr>
<td>RCA Clean</td>
<td>40</td>
<td>40</td>
<td>Clean</td>
</tr>
</tbody>
</table>
## COST OF OWNERSHIP FOR RIT TOOLS

<table>
<thead>
<tr>
<th>Tool</th>
<th>Cost Per Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVC 601 Sputtering System</td>
<td>$54.41</td>
</tr>
<tr>
<td>GCA 9001 Coat or Develop Line</td>
<td>$82.71</td>
</tr>
<tr>
<td>GCA Stepper</td>
<td>$77.85</td>
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<tr>
<td>Asher</td>
<td>$54.83</td>
</tr>
<tr>
<td>Varian 400 Ion Implanter</td>
<td>$112.00</td>
</tr>
<tr>
<td>Bruce Furnace</td>
<td>$55.81</td>
</tr>
<tr>
<td>RCA Clean</td>
<td>$30.97</td>
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<tr>
<td>LPCVD</td>
<td>$44.38</td>
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<tr>
<td>RIE</td>
<td>$110.34</td>
</tr>
<tr>
<td>Wet Etch</td>
<td>$49.28</td>
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</tbody>
</table>

Using These Numbers the Cost/wafer for CMOS PW-4 Wafers is $5861/wafer (compared to $1000/wafer for industry)
## EQUIPMENT UTILIZATION STUDY

<table>
<thead>
<tr>
<th>Tool</th>
<th>Idle</th>
<th>Lab</th>
<th>Factory</th>
<th>Research</th>
<th>Maintenance</th>
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</thead>
<tbody>
<tr>
<td>CVC 601 Sputtering System</td>
<td>83%</td>
<td>3%</td>
<td>1%</td>
<td>13%</td>
<td>0%</td>
</tr>
<tr>
<td>GCA 9001 Wafertrac</td>
<td>72%</td>
<td>17%</td>
<td>2%</td>
<td>9%</td>
<td>0%</td>
</tr>
<tr>
<td>GCA Stepper</td>
<td>72%</td>
<td>17%</td>
<td>2%</td>
<td>9%</td>
<td>0%</td>
</tr>
<tr>
<td>Asher</td>
<td>89%</td>
<td>1%</td>
<td>3%</td>
<td>5%</td>
<td>2%</td>
</tr>
<tr>
<td>Varian 400 Ion Implanter</td>
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<td></td>
<td></td>
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<tr>
<td>Furnace 12 Gate Oxide</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>RCA Clean</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPCVD</td>
<td>54%</td>
<td>0%</td>
<td>2%</td>
<td>41%</td>
<td>3%</td>
</tr>
</tbody>
</table>
RESULTS

§ The Goals of the Factory Have Been Met

§ Students do know how to do all unit processes (operate all tools used in the CMOS process, and understand what and why they are doing what they do)
§ Students learn about WIP tracking, CIM, Cycle Time Management, Real Time SPC, Six Sigma and TQM Methodologies
§ A CMOS Foundry Service is Available

§ The Laboratory has Benefited in that:

§ We have excellent instruction sets, operation manuals, log sheets and maintenance logs
§ The CIM system has been developed to provide WIP tracking, Instructions, Data Collection and Lot History
§ The baseline CMOS process has been maintained and works
FUTURE WORK

§ Continuous Improvement
§ More Automation
§ Better Modeling of Factory Performance and Verification
§ 150mm wafers and required process changes
§ Advance processes can be done by the student factory including:
  §§ Submicron transistor integrated circuits
  §§ Bi CMOS processes
  §§ Microelectromechanical device processes
CONCLUSION

- The CIM System is essential for a project such as this
- Very interesting project
- Useful as an educational tool
  - SPC
  - TQM
  - 6 σ
  - Microelectronics Manufacturing Engineering
- Open Ended Project
HOMEWORK - FACTORY

1. What is the main purpose of the student run factory?
2. What does acronym MESA stand for?
3. What does the Operator User Interface allow the operator do in MESA?
4. What processes and products are used/made in the RIT student factory?
5. Which lots are selected first for processing in the RIT student factory?
6. What is an approximate value for daily wafer moves in RIT’s factory? In industry?
7. What is cycle time? How is it measured?
8. Calculate the value for Cp, k, and Cpk for the following set of measured oxide thickness given the target of 5000 Å, USL of 5500 Å and LSL of 4500 Å
   (4958, 4848, 5025, 4772, 4779, 4558, 4623, 4973, 4884, 4866, 5075, 5871, 4981, 4842, 4612, 5214, 5243, 4323, 4905, 5449, 4035, 5243, 4282, 4097, 4941, 4846)
9. What is the most recent value (in these notes) for Cpk for gate oxide?
10. What does it cost to process a CMOS wafer at RIT? In industry?