Introduction to VLSI

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INTRODUCTION TO VLSI

OUTLINE

Introduction
Process Technology
Digital Electronics
  Inverter with Resistor Load
  CMOS Inverter
  Voltage Transfer Curve (VTC)
  Noise Margins, Rise/Fall Time
MOSIS Layout Design Rules
Standard Cell Design
  Primitive, Basic, Macro Cells
Maskmaking
References
Homework
VLSI is an acronym for Very Large Scale Integration. This includes Integrated circuits with greater than tens of thousands of transistors including multi-million or even billions of transistors.

VLSI Design refers to methodologies and computer software tools for designing digital circuits with huge numbers of transistors. Some of these methodologies and tools can also be applied to analog circuit design.

Software tools include schematic capture, SPICE analog simulation, switch level digital simulation, layout editors, layout versus schematic checking, design rule checking (DRC), auto place and routing and many more.
Computer software is used to check the layout, compare the layout to the schematic and make it possible to design circuits with millions of transistors with no errors.
VLSI DESIGN METHODOLOGIES

Full Custom Design
Direct control of layout and device parameters
Longer design time
High performance
fast, low power, dense

Standard Cell Design
Easy to implement
Medium performance
Limited cell library selections

Gate Array or
Programmable Logic Array Design
Fastest design turn around
Process Technology
It is not necessary to know all process details to do CMOS integrated circuit design. However the process determines important circuit parameters such as supply voltage and maximum frequency of operation. It also determines if devices other than PMOS and NMOS transistors can be realized such as poly-to-poly capacitors and EEPROM transistors. The number of metal interconnect layers is also part of the process definition. Starting wafer type determines if isolated n-wells or p-wells are available.
RIT PROCESSES

At RIT we use the Sub-CMOS and ADV-CMOS processes for most designs. In these processes the minimum poly length is 1µm and 0.5µm respectively. We use scalable MOSIS design rules with lambda equal to 0.5µm and 0.25µm. These processes use one layer of poly and two layers of metal.

The examples on the following pages are designs that could be made with either of the above processes. As a result the designs are generous, meaning that larger than minimum dimensions are used. For example $\lambda = 0.5\mu m$ and minimum poly is $2\lambda$ but designed at 2.5µm because our poly etch is isotropic.

The design approach for digital circuits is to design primitive cells and then use the primitive cells to design basic cells which are then used in the project designs. A layout approach is also used that allows for easy assembly of these cells into more complex cells.
RIT Subμ CMOS

150 mm wafers
Nsub = 1E15 cm⁻³
Nn-well = 3E16 cm⁻³
Xj = 2.5 μm
Np-well = 1E16 cm⁻³
Xj = 3.0 μm
LOCOS
Field Ox = 6000 Å
Xox = 150 Å
Lmin = 1.0 μm
LDD/Side Wall Spacers
2 Layers Aluminum

3.3 Volt Technology
VT’s = +/- 0.75 Volt
Robust Process (always works)
Fully Characterized (SPICE)
RIT SUBμ CMOS

Substrate 10 ohm-cm

NMOSFET
PMOSFET

N+ Poly
5000 Å Field Oxide
P+ D/S
N+ D/S
LDD
N+ D/S
LDD
p+ well contact
n+ well contact
Channel Stop
RIT Advanced CMOS

150 mm Wafers
Nsub = 1E15 cm\(^{-3}\) or 10 ohm-cm, p
Nn-well = 1E17 cm\(^{-3}\)
Xj = 2.5 \(\mu m\)
Np-well = 1E17 cm\(^{-3}\)
Xj = 2.5 \(\mu m\)
Shallow Trench Isolation
Field Ox (Trench Fill) = 4000 Å
Dual Doped Gate n+ and p+
Xox = 100 Å
Lmin = 0.5 \(\mu m\) , Lpoly = 0.35 \(\mu m\), Leff = 0.11 \(\mu m\)
LDD/Nitride Side Wall Spacers
TiSi2 Salicide
Tungsten Plugs, CMP, 2 Layers Aluminum

Vdd = 3.3 volts
Vto=+- 0.75 volts
Digital Electronics
**INVERTER**

**SYMBOL**

VIN → O → VOUT

**TRUTH TABLE**

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**SWITCH**

VIN → O → VOUT

**RESISTOR**

VIN → O → VOUT

**LOAD**

VIN → O → VOUT
NML, noise margin low, $\Delta 0 = V_{iL} - V_{oL}$

NMH, noise margin high, $\Delta 1 = V_{oH} - V_{iH}$
LTSPICE - INVERTER VTC – FOR DIFFERENT RL

R=1K

VTC for different RPs

R=5K

R=10K

IBM
OTHER INVERTER TYPES - VOUT VS VIN (VTC)

- NMOS ENHANCEMENT LOAD
- CMOS
- PMOS ENHANCEMENT LOAD
- NMOS ENHANCEMENT LOAD
- NMOS DEPLETION LOAD
CMOS INVERTER

VIN — VOUT

Idd

CMOS

NML, noise margin low, $\Delta O = V_{iL} - V_{oL}$

NMH, noise margin high, $\Delta 1 = V_{oH} - V_{iH}$
LTSPICE – CMOS INVERTER
INVERTER PROPERTIES

DC Properties
  Noise Margins
  Current, $I$
  Size

Transient Properties
  Rise/Fall Time
  Fan Out
RISE TIME AND FALL TIME LTSPICE SIMULATION

The LTSPICE simulation shows the rise time and fall time of a circuit. The graphs display the voltage (Vout3 and Vout1) over time, with key times labeled:
- Rise time:
  - 0.13ns
  - 18.6ns
  - 132.16ns
  - 161.48ns
- Fall time:
  - 22.26ns
  - 59.65ns
  - 110.02ns
  - 120.85ns

The circuit diagram includes components such as resistors (R1, R2) and capacitors (C1, C2). The simulation parameters are set with .tran .2u .op and include the file c:\SPICE\RIT_Models_For_LTSPICE.txt.

PULSE(0 5 0 0 0 .1u .2u 5)
**NOR GATE**

**Symbol**

**Truth Table**

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**Diagram**

Switch

Resistor Load

CMOS
**NAND GATE**

**SYMBOL**

```
+V
R
VA
VB
```

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**R**

```
R
V
```

**SWITCH**

```
VA
VB
```

**RESISTOR**

```
V
```

**LOAD**

```
VA
```

**CMOS**

```
V
```

```
VA
VB
```

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**Microelectronic Engineering**

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OTHER LOGIC GATES

**AND**

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**OR**

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ADDITION IN BINARY

IN BASE 10

7
+2
___
9

IN BINARY

11 CARRY
0111
0010
___
1001 SUM

TRUTH TABLE
FOR ADDITION
RULES

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### AND-OR CIRCUIT REALIZATION OF SUM

#### TRUTH TABLE FOR ADDITION RULES

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</table>

- **A**: One input to the AND gate.
- **B**: Another input to the AND gate.
- **CIN**: Carry from the previous stage.
- **SUM**: Output from the AND gate.
- **COUT**: Output from the OR gate.
CIRCUIT REALIZATION OF CARRY OUT (COUT)

TRUTH TABLE FOR ADDITION RULES

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**FILP-FLOPS**

**RS FLIP FLOP**

\[ R \quad Q \]

\[ S \quad QBAR \]

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**D FLIP FLOP**

\[ \text{DATA} \quad \text{CLOCK} \]

\[ Q \quad QBAR \]

\[ Q = \text{DATA IF CLOCK IS HIGH} \]

\[ \text{IF CLOCK IS LOW } Q = \text{PREVIOUS DATA VALUE} \]
**MASTER-SLAVE D FLIP FLOP**

![Diagram of the master-slave D flip flop](image)

**NEGATED INPUT NOR IS EQUAL TO AND**

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<th>(\bar{B})</th>
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Microelectronic Engineering

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ALL NOR MASTER SLAVE D FLIP FLOP
AND-OR realizations are easily derived from truth table description of a circuits performance. Replacing the AND and OR gates with all NOR gates is equivalent. Replacing the AND and OR gates with all NAND gates is equivalent.
CIRCUIT REALIZATION FOR XOR

Exclusive OR
XOR

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Layout Design Rules
The design rules may change from foundry to foundry or for different technologies. So to make the design rules generic the sizes, separations and overlap are given in terms of numbers of lambda ($\lambda$). The actual size is found by multiplying the number by the value for lambda for that specific foundry.

For example:

RIT PMOS process $\lambda = 10 \ \mu m$ and minimum metal width is $3 \ \lambda$ so that gives a minimum metal width of $30 \ \mu m$. The RIT SUB-CMOS process has $\lambda = 0.5 \ \mu m$ and the minimum metal width is also $3 \ \lambda$ so minimum metal is $1.5 \ \mu m$ but if we send our CMOS designs out to industry $\lambda$ might be $0.25 \ \mu m$ so the minimum metal of $3 \ \lambda$ corresponds to $0.75 \ \mu m$. In all cases the design rule is the minimum metal width $= 3 \ \lambda$. 
We will use a modified version of the MOSIS TSMC 0.35 2P 4M design rules. Eventually we hope to be compatible with MOSIS but new process technology needs to be developed at RIT to do that (PECVD Tungsten, 4 layer metal). We use one layer of poly and two layers of metal. We will use the same design layer numbers with additional layers as defined on the following pages for manufacturing/maskmaking enhancements. Many of the designs will use minimum drawn poly gate lengths of 2µm where circuit architecture is the main purpose of the design. Minimum size devices (Drawn Poly = 0.5µm, etc.) are included to develop manufacturing process technology. These transistors (0.5µm drawn) yield 0.35µm $L_{eff}$ and are equivalent to the TSMC 0.35µm transistors.
**LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L**

- **Lamb**da = design rule parameter, $\lambda$, ie $0.25\mu$m
- L**min** = min drawn poly length, $2\lambda$ $0.50\mu$m
- L**mask** = ? Depends on +/- bias $1.00\mu$m x 5
- L**poly** after poly etch $0.40\mu$m
- L**poly** after poly reoxidation $0.35\mu$m
- L**drawn** = what was drawn
- L**int** = distance between junctions, including under diffusion $0.30\mu$m
- L**eff** = distance between space charge layers, $V_d = V_s = 0$ $0.20\mu$m
- L = distance between space charge layers, when $V_d$ = what it is $0.11\mu$m

**Internal Channel Length**, L**int** = distance between junctions, including under diffusion

**Effective Channel Length**, L**eff** = distance between space charge layers, $V_d = V_s = 0$

**Channel Length**, L = distance between space charge layers, when $V_d$ = what it is

**Extracted Channel Length Parameters** = anything that makes the fit good (not real)
**MOSIS TSMC 0.35 2POLY 4 METAL PROCESS**


**MOSIS SCMCOS Technology Codes and Layer Maps**

**SCN4M and SCN4M_SUBM**

This is the layer map for the technology codes SCN4M and SCN4M_SUBM using the MOSIS Scalable CMOS layout rules (SCMOS), and only for SCN4M and SCN4M_SUBM. For designs that are laid out using other design rules (or technology codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

**SCN4M**: Scalable CMOS N-well, 4 metal, 1 poly, silicided. Silicide block and thick oxide option available only on the TSMC process.

**SCN4M_SUBM**: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Fabricated on TSMC, AMIS, and Agilent/HP 0.35 micron process runs. See "Notes" section of layer map for foundry-specific options.

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<th>CIF Suffix</th>
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<th>Notes</th>
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<td>CTA</td>
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<td>24</td>
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<td>CSB</td>
<td></td>
<td>20</td>
<td>Optional for Agilent/HP; not available for AMI</td>
</tr>
<tr>
<td>N_PLUS_SELECT</td>
<td>45</td>
<td>CNS</td>
<td></td>
<td>4</td>
<td></td>
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<tr>
<td>P_PLUS_SELECT</td>
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<td></td>
<td>4</td>
<td></td>
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<tr>
<td>CONTACT</td>
<td>25</td>
<td>CCC</td>
<td>CCG</td>
<td>5, 6, 13</td>
<td>Can be replaced by CONTACT</td>
</tr>
<tr>
<td>POLY_CONTACT</td>
<td>47</td>
<td>CCP</td>
<td></td>
<td>8</td>
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</tr>
<tr>
<td>ACTIVE_CONTACT</td>
<td>48</td>
<td>CCA</td>
<td></td>
<td>6</td>
<td>Can be replaced by CONTACT</td>
</tr>
<tr>
<td>METAL1</td>
<td>49</td>
<td>CM1</td>
<td>CMF</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>VIA</td>
<td>50</td>
<td>CV1</td>
<td>CVA</td>
<td>8</td>
<td></td>
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<tr>
<td>METAL2</td>
<td>51</td>
<td>CM2</td>
<td>CMS</td>
<td>9</td>
<td></td>
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<tr>
<td>VIA2</td>
<td>61</td>
<td>CV2</td>
<td>CVB</td>
<td>14</td>
<td></td>
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<tr>
<td>METAL3</td>
<td>62</td>
<td>CM3</td>
<td>CMT</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>VIA3</td>
<td>30</td>
<td>CV3</td>
<td>CVT</td>
<td>21</td>
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<tr>
<td>METAL4</td>
<td>31</td>
<td>CM4</td>
<td>CMQ</td>
<td>22</td>
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</tr>
<tr>
<td>GLASS</td>
<td>52</td>
<td>CQG</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>PADS</td>
<td>26</td>
<td>XP</td>
<td></td>
<td></td>
<td>Non-fab layer used to highlight pads</td>
</tr>
<tr>
<td>Comments</td>
<td>--</td>
<td>CX</td>
<td></td>
<td></td>
<td>Comments</td>
</tr>
</tbody>
</table>

| TSMC          | 0.35 micron | 2P4M (4 Metal Polycided, 3.3 V/5 V) | 0.25 | SCN4ME |

© May 7, 2015  Dr. Lynn Fuller
### MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

<table>
<thead>
<tr>
<th>MASK LAYER NAME</th>
<th>MENTOR NAME</th>
<th>GDS #</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>N WELL</td>
<td>N_well.i</td>
<td>42</td>
<td></td>
</tr>
<tr>
<td>ACTIVE</td>
<td>Active.i</td>
<td>43</td>
<td></td>
</tr>
<tr>
<td>POLY</td>
<td>Poly.i</td>
<td>46</td>
<td></td>
</tr>
<tr>
<td>N PLUS</td>
<td>N_plus_select.i</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>P PLUS</td>
<td>P_plus_select.i</td>
<td>44</td>
<td></td>
</tr>
<tr>
<td>CONTACT</td>
<td>Contact.i</td>
<td>25</td>
<td>Active_contact.i 48</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>poly_contact.i 47</td>
</tr>
<tr>
<td>METAL1</td>
<td>Metal1.i</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>VIA</td>
<td>Via.i</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>METAL2</td>
<td>Metal2.i</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>VIA2</td>
<td>Via2.i</td>
<td>61</td>
<td>Under Bump Metal</td>
</tr>
<tr>
<td>METAL3</td>
<td>Metal3.i</td>
<td>62</td>
<td>Solder Bump</td>
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</table>

These are the main design layers up through metal two.
### MORE LAYERS USED IN MASK MAKING

<table>
<thead>
<tr>
<th>LAYER</th>
<th>NAME</th>
<th>GDS</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>cell_outline.i</td>
<td>70</td>
<td>Not used</td>
</tr>
<tr>
<td></td>
<td>alignment</td>
<td>81</td>
<td>Placed on first level mask</td>
</tr>
<tr>
<td></td>
<td>nw_res</td>
<td>82</td>
<td>Placed on nwell level mask</td>
</tr>
<tr>
<td></td>
<td>active_lettering</td>
<td>83</td>
<td>Placed on active mask</td>
</tr>
<tr>
<td></td>
<td>channel_stop</td>
<td>84</td>
<td>Overlay/Resolution for Stop Mask</td>
</tr>
<tr>
<td></td>
<td>pmos_vt</td>
<td>85</td>
<td>Overlay/Resolution for Vt Mask</td>
</tr>
<tr>
<td></td>
<td>LDD</td>
<td>86</td>
<td>Overlay/Resolution for LDD Masks</td>
</tr>
<tr>
<td></td>
<td>p plus</td>
<td>87</td>
<td>Overlay/Resolution for P+ Mask</td>
</tr>
<tr>
<td></td>
<td>n plus</td>
<td>88</td>
<td>Overlay/Resolution for N+ Mask</td>
</tr>
<tr>
<td></td>
<td>tile_exclusion</td>
<td>89</td>
<td>Areas for no STI tiling</td>
</tr>
</tbody>
</table>

These are the additional layers used in layout and mask making.
**MOSIS LAMBDA BASED DESIGN RULES**

http://www.mosis.com/design/rules/

If $\lambda = 1 \, \mu m$ then contact is $2 \, \mu m \times 2 \, \mu m$
MOSIS LAMBDA BASED DESIGN RULES

http://www.mosis.com/design/rules/

MOSIS Educational Program

Instructional Processes Include:
AMI $\lambda = 0.8 \mu m$ SCMOS Rules
AMI $\lambda = 0.35 \mu m$ SCMOS Rules

Research Processes:
go down to poly length of 65nm
MOSIS REQUIREMENTS

MOSIS requires that projects have successfully passed LVS (Layout Versus Schematic) and DRC (Design Rule Checking). The MENTOR tools for LVS and DRC (as they are set up at RIT) require separate N-select and P-select levels in order to know an NMOS transistor from a PMOS transistor. Although either an N-well, P-well or both will work for a twin well process, we have set up our DRC to look for N-well. (Also since we use a p-type starting wafer we can not have isolated p-wells but we can have isolated n-wells, thus drawing separate n-wells can be useful for some circuit designs.)

http://www.mosis.com
Digital Circuit Layout
The design approach for digital circuits is to design primitive cells and then use the primitive cells to design basic cells which are then used in the project designs. A layout approach is also used that allows for easy assembly of these cells into more complex cells.

**Primitive Cells**
- INVERTER, NAND2,3,4, NOR2,3,4, NULL

**Basic Cells**
- XOR, MUX, DEMUX, ENCODER, DECODER
- FULL ADDER, FLIP FLOPS

**Macro Cells**
- BINARY COUNTER
- SRAM
**LAYOUT – GATE ARRAY**

Green is Active
Dashed Yellow is N-Well
Red is Poly
Blue is Metal-One
Pink is Metal-Two
White is Contact Cut
Yellow is Via
P and N select not shown
1. Cells are separated from adjacent cells by off transistors
2. Well contacts are made at each of the off transistors
3. Metal-two connects thru Via to Metal-one
4. Metal-one connects thru Contact Cuts to active and Poly
5. Inputs and Outputs connections are made vertically with Metal-two
6. Routing channels exist above and below the gate array and contain horizontal metal-one interconnects between cells, with Via to Metal-two.
7. The NULL cell at the end of the gate array row satisfy design rules for extension of well beyond active, etc. It also provides a vertical routing channel which may be useful in constructing macro cells.
INVERTER

Vin — Vout

PMOS

NMOS

Vin — Vout

+V

Idd

CMOS

TRUTH TABLE

<table>
<thead>
<tr>
<th>VIN</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.0µm
Leff = 0.35 µm
**INVERTER**

- $W = 40 \, \mu m$
- $L_{\text{drawn}} = 2.5 \, \mu m$
- $L_{\text{poly}} = 1.0 \, \mu m$
- $L_{\text{eff}} = 0.35 \, \mu m$
PRIMITIVE CELLS
VERIFICATION NOR2 NAND3 FABRICATION & TEST

NOR2

Output

Graph Display

Setting the input terminals

NAND3

Output

A Low High Low High Low Low Low Low
B Low Low High High Low Low Low Low
C Low Low Low Low Low Low Low Low

A Low High Low High Low High Low Low Low
B Low Low High High Low High Low Low Low
C Low Low Low Low Low Low Low Low
BASIC DIGITAL CELLS WITH PADS

Multiplexer  XOR  Full Adder  Encoder  Decoder  Demux

Edge Triggered D FF  JK FF

Rochester Institute of Technology
Microelectronic Engineering
**BASIC CELL XOR**

**Input A**
- Port in
- \( A' \)
- \( A'B \)

**Input B**
- Port in
- \( B \)
- \( A \)
- \( AB' \)

**Equation:**
\[
\text{XOR} = A'B + AB'
\]

**Port out**
XOR

---

**Microelectronic Engineering**
Rochester Institute of Technology
FULL ADDER

A

B

Cin

SUM

null nand4 nand3 nand3 nand3 inverter inverter nand3 nand3 nand3 nand3 nand3 nand4 null
1 TO 4 DEMULTIPLEXER

Correct

Rochester Institute of Technology
Microelectronic Engineering
DECODER

A → Q₀
B → Q₁
B → Q₂
B → Q₃

Correct
Digital Encoder

512 inputs can be coded into 9 lines which is a more dramatic benefit

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>Q0</th>
<th>Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
EDGE TRIGGERED D TYPE FLIP FLOP

Positive Edge Triggered
D FF

Inputs | Outputs
---|---
D | Q' Q
0 | 0 1
1 | 1 0
X | Q Q
X | Q Q

CLK

Rochester Institute of Technology
Microelectronic Engineering
**JK FLIP FLOP**

**Positive Edge Triggered JK FF**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>J K C</td>
<td>Q Q'</td>
</tr>
<tr>
<td>0 0 ↑</td>
<td>Q Q</td>
</tr>
<tr>
<td>0 1 ↑</td>
<td>1 1</td>
</tr>
<tr>
<td>1 0 ↑</td>
<td>Q Q'</td>
</tr>
<tr>
<td>1 1 ↑</td>
<td>Q Q</td>
</tr>
<tr>
<td>X X 0</td>
<td>Q Q'</td>
</tr>
<tr>
<td>X X 1</td>
<td>Q Q'</td>
</tr>
</tbody>
</table>
T-TYPE FILP-FLOP

TOGGLE FLIP FLOP

\[ T \]

Q

QBAR

\( Q: \) Toggles High and Low with Each Input

<table>
<thead>
<tr>
<th>T</th>
<th>Qn-1</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
BINARY COUNTER USING T TYPE FLIP FLOPS

State Table for Binary Counter

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>F-F Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A  B  C</td>
<td>A  B  C</td>
<td>T_A  T_B  T_C</td>
</tr>
<tr>
<td>0  0  0</td>
<td>0  0  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>0  0  1</td>
<td>0  1  0</td>
<td>0  1  1</td>
</tr>
<tr>
<td>0  1  0</td>
<td>0  1  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>0  1  1</td>
<td>1  0  0</td>
<td>1  1  1</td>
</tr>
<tr>
<td>1  0  0</td>
<td>1  0  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>1  0  1</td>
<td>1  1  0</td>
<td>0  1  1</td>
</tr>
<tr>
<td>1  1  0</td>
<td>1  1  1</td>
<td>0  0  1</td>
</tr>
<tr>
<td>1  1  1</td>
<td>0  0  0</td>
<td>1  1  1</td>
</tr>
</tbody>
</table>

Input Pulses

TOGGLE FLIP FLOP

T  Qn-1  Q
0  0  0
0  1  1
1  0  1
1  1  0

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Page 62
3-BIT BINARY COUNTER WITH D FLIP FLOPS
MACROCELLS

Binary Counter
SRAM
3-BIT BINARY COUNTER/SHIFT REGISTER

Binary Counter
Serial Output
Asynchronous Reset
Count Up Enable
Shift Out Clock Input
Count Up Clock Input
Start Bit and Stop Bit
ADDITIONAL CIRCUITRY TO RESET, SHIFT, COUNT
Maskmaking
This process can take weeks and cost between $1000 and $20,000 for each mask depending on the design complexity.
**OTHER MASKMAKING FEATURES**

- Fiducial Marks: marks on the edge of the mask used to align the mask to the stepper
- Barcodes
- Titles
- Alignment Keys: marks on the wafer from a previous level used for wafer alignment
- CD Resolution Targets: lines and spaces
- Overlay Verniers: structures that allow measurement of x and y overlay accuracy
- Tiling
- Optical Proximity Correction (OPC)
MEBES - Manufacturing Electron Beam Exposure System
ASML RETICLE

Chrome Side
Mirrored 90°
Chip Bottom at Bottom

Non Chrome Side
As loaded into Reticle Pod,
Chrome Down, Reticle Pre-
Alignment Stars Sticking out
of Pod
NA = 0.48 to 0.60 variable
σ = 0.35 to 0.85 variable
With Variable Kohler, or
Variable Annular illumination
Resolution = K1 λ/NA
= ~ 0.35μm
for NA=0.6, σ = 0.85
Depth of Focus = k₂ λ/(NA)²
= > 1.0 μm for NA = 0.6

i-Line Stepper λ = 365 nm
22 x 27 mm Field Size
RIT SUB-CMOS PROCESS

NMOSFET  PMOSFET

N+ Poly  0.75 µm Aluminum

N+ D/S  LDD

P+ well  n+ well contact

Channel Stop

N-type Substrate 10 ohm-cm

LVL 1 – n-WELL
LVL 2 - ACTIVE
LVL 3 - STOP
LVL 4 - PMOS VT
LVL 5 - POLY
LVL 6 – P-LDD
LVL 7 – N-LDD
LVL 8 - P+ D/S
LVL 8 - CC
LVL 9 - N+ D/S
LVL 9 - METAL

11 PHOTO LEVELS
RIT ADVANCED CMOS

12 PHOTO LEVELS + 2 FOR EACH ADDITIONAL METAL LAYER
FILE FORMATS

Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only
REFERENCES

1. Do a SPICE simulation to obtain the VTC for the inverter shown on page 16. Let the load resistor be 10K, the NMOS transistor SPICE model RITSUBN7, $L=1\mu\text{m}$ and $W=40\mu\text{m}$. Extract $V_{OH}$, $V_{OL}$, $V_{IL}$, $V_{IH}$, $V_{INV}$, Noise Margin Low, Noise Margin High and Maximum current.

2. Do a SPICE simulation to obtain the VTC for the inverter shown on page 20. Let the NMOS and PMOS transistor SPICE model RITSUBN7 and RITSUBP7, $L=1\mu\text{m}$ and $W=40\mu\text{m}$. Extract $V_{OH}$, $V_{OL}$, $V_{IL}$, $V_{IH}$, $V_{INV}$, Noise Margin Low, Noise Margin High and Maximum current.

3. Do a SPICE simulation to obtain the RISE TIME and FALL TIME for the inverter in problem 2 with a load capacitance equal to a fan out of 5 gates.

4. Show that the XOR realized with AND and OR gates is equivalent to an all NAND gate realization.
TRANSISTOR DIMENSIONS

\[ L = 2 \mu \]
\[ W = 40 \mu \]
\[ A_d = A_s = 40 \mu \times 17 \mu = 680 \text{p} \]
\[ P_d = P_s = 2 \times (40 \mu + 17 \mu) = 114 \mu \]
\[ R_d = R_s = 100 \text{ ohm} \]