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SPICE (Simulation Program for Integrated Circuit Engineering) is a general-purpose circuit simulation program for non-linear DC, non-linear transient, and linear AC analysis. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and several semiconductor devices: including diodes, BJT s, JFETs, MESFETs, and MOSFETs. Circuits with large numbers of all types of components can be simulated. You can think of SPICE as a nodal network solver that outputs all the node voltages and branch currents. One node must be named “0” (the ground node) and is the reference node for all the node voltages.

SPICE input files and output files are simple text files (e.g. name.txt)

Input files include a TITLE, circuit description NET LIST, analysis directives (COMMANDS), and lists of other text files to include (INC) such as model libraries (LIB) and an .END command.
**INTRODUCTION**

LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSPICE Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components. (This is a good choice for your home computer.)

The input file for SPICE is generated automatically from the schematic capture software. In the old days the input file was created by hand as a simple text file. SPICE can still run using a simple text file as the input but today most users prefer to use schematic capture software to create the input file.

These files are read line by line. If the line starts with “#” it is a comment and what follows on that line is ignored. SPICE directives start with a “.” such as .END or .INCLUDE path\folder\filename.txt or .MODEL modelname NMOS (Level=7 etc etc etc.....) Upper and Lower case are treated the same (not case sensitive) thus m stands for milli, and MEG stands for mega.
MOSFET Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, Level 7, Level 8, Level 49, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.

In general first generation models are recommended for MOSFETs with gate lengths of 10um or more. If not specified most SPICE MOSFET Models default to level=1 (Shichman and Hodges)
Unless the gate length is 10um or larger we should use third generation models.
This is a measured IDS – VDS family of curves for a two micrometer gate length (16um width) NMOS FET.
Using SPICE to generate the IDS – VDS family of curves with level 1 or level 2 models do not give good results. Note current levels in Level=1 is wrong and the shape is not correct in either simulation.
This page documents how to include correct SPICE MOSFET properties or attributes. The model RITSUBN7 is not in any LTSPICE library so its location needs to be given. See how to do that on the next page.
This is how you let LTSPICE know where to find the RITSUBN7 model.
This shows a text file with SPICE models for a diode, NMOS, PMOS and NPN BJT.
This is the resulting simulation of IDS – VDS when using the correct spice model. More details are given in the video on Dr. Fullers webpage.
Comparison of measured and simulated IDS – VDS family of curves.
Comparison of Level 1 and Level 7 simulations (in Green) to the measured curves (in Yellow).
In addition to the family of curves we also want the simulated Id-Vgs sweep and subthreshold characteristics to match the measured curves. (in Yellow) This slide shows the measured Id-Vgs sweep and the derivative (which is gm – transconductance). Note that a level=1 MOSFET SPICE model is totally wrong.
This shows a third generation MOSFET SPICE model simulation of Id-Vgs and gm. It is correct.
This shows a third generation MOSFET SPICE model simulation of the subthreshold characteristics. It is correct.
This slide shows a symbol, circuit schematic and theoretical Vout vs Vin (Voltage Transfer Curve – VTC) for a CMOS inverter. The definitions of ViL, VoL, VoH and ViH are shown at the points where the VTC plot has a slope of minus one. These are used to calculate the delta zero and delta one noise margins. The noise margins are evaluated as part of the inverter figure of merit. Other parameters include maximum current during switching, gain, gate delay and more.
This slide shows an RIT fabricated CMOS inverter VTC and I vs Vin.
This slide shows the layout for the RIT inverter (measured results shown on previous slide). From the layout the transistor length and widths are extracted. So L=1.5µm and W=40µm. Leff is less than poly but will be calculated by SPICE from the model parameters.
This is a SPICE simulated VTC, Gain and I vs Vin. The shape is correct but the simulated current is higher than the measured current. There could be many reasons for this discrepancy including not enough data when measuring only one device. From these curves data can be extracted for Gain, Imax and noise margins which can be compared to the measured values.
Conclusion – use third generation models such as LEVEL = 7 or LEVEL = 8
The ring oscillator is used to measure the gate delay. A large number (odd number) of inverters are connected in a ring. Once power is applied it will oscillate with a period of $T$ equal to 2 times $N$ times $td$. The other two inverters shown are buffers so that the scope probe will not slow the oscillation with its capacitance (~15pF). Using a large number of inverters slows the frequency of oscillation thus the oscilloscope need not be a high frequency special oscilloscope.
This is a photograph of the 73 stage ring oscillator and a capture of the measured output voltage. The period is 104 ns which gives an individual inverter gate delay of 718 ps with a 5 V supply voltage.
To model the ring oscillator correctly all the internal resistors and capacitors need to be defined. They are defined with a combination transistor attributes and spice model.
This slide shows the definitions of the internal resistors and capacitors. Also shown are the transistor parameters that are combined with the SPICE parameters.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS,RS</td>
<td>Source/Drain Series Resistance, ohms</td>
</tr>
<tr>
<td>RSH</td>
<td>Sheet Resistance of Drain/Source, ohms</td>
</tr>
<tr>
<td>CGSO,CGDO</td>
<td>Zero Bias Gate-Source/Drain Capacitance, F/m of width</td>
</tr>
<tr>
<td>CGBO</td>
<td>Zero Bias Gate-Substrate Capacitance, F/m of length</td>
</tr>
<tr>
<td>CJ</td>
<td>DS Bottom Junction Capacitance, F/m2</td>
</tr>
<tr>
<td>CJSW</td>
<td>DS Side Wall Junction Capacitance, F/m of perimeter</td>
</tr>
<tr>
<td>MJ</td>
<td>Junction Grading Coefficient, 0.5</td>
</tr>
<tr>
<td>MJSW</td>
<td>Side Wall Grading Coefficient, 0.5</td>
</tr>
</tbody>
</table>

These are combined with the transistors parameters (attributes):
- L, W: Length and Width
- AS, AD: Area of the Source/Drain
- PS, PD: Perimeter of the Source/Drain
- NRS, NRD: Number of squares Contact to Channel
Our test chip has five different ring oscillators. The 73 stage layout is shown.
This is a close up of the inverter transistors in the 73 stage ring oscillator. The rulers that were added help in determining the dimensions.
The measured dimensions are shown here. In LTSPICE use Ctrl Right Click and enter the dimensions. To see the dimensions on the schematic place an X in the right column by double click.

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>2u</td>
<td>2u</td>
</tr>
<tr>
<td>W</td>
<td>12u</td>
<td>30u</td>
</tr>
<tr>
<td>AD</td>
<td>12ux12u=144p</td>
<td>12ux30u=360p</td>
</tr>
<tr>
<td>AS</td>
<td>12ux12u=144p</td>
<td>12ux30u=360p</td>
</tr>
<tr>
<td>PD</td>
<td>2x(12u+12u)=48u</td>
<td>2x(12u+30u)=84u</td>
</tr>
<tr>
<td>PS</td>
<td>2x(12u+12u)=48u</td>
<td>2x(12u+30u)=84u</td>
</tr>
<tr>
<td>NRS</td>
<td>1</td>
<td>0.3</td>
</tr>
<tr>
<td>NRD</td>
<td>1</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Use Ctrl right Click on all NMOS and all PMOS. Then enter these values. Double click in right column X means values will be displayed on schematic.
This is a OrCAD PSPICE schematic and the simulated output. The simulation gives 1096 ps for gate delay and the measured gate delay is 718ps. This is a good result.
Conclusion

Since the measured and the simulated gate delays, $t_d$ are close to correct, then the SPICE model must be close to correct. The inverter gate delay depends on the values of the internal capacitors and resistances of the transistor.

Specifically:
- $RS$, $RS$, $RSH$
- $CGSO$, $CGDO$, $CGBO$
- $CJ$, $CJSW$

These are combined with the transistors
- $L$, $W$  Length and Width
- $AS$, $AD$  Area of the Source/Drain
- $PS$, $PD$  Perimeter of the Source/Drain
- $NRS$, $NRD$  Number of squares Contact to Channel
The output plots can be changed so that the background is white instead of default black. Two cursors can be placed on a plot and the x-y value, difference and slope is given in a pop up data box. Other useful tools include “copy as a bitmap to clipboard”.

Colors can be set using the tools menu on the top banner.

A cursor can be set by left click on trace name at top of the waveform. The x and y location of the cursor will be displayed.

A second cursor can be set up by right click on the trace name. The x and y location of both cursors will be displayed along with the differences and slope.

Tools also provides for copy of bitmap to clipboard function.
Cursors can be added to the waveform.
Tools also allow other colors to be changed. Here I show the axis changed from grey to black. On the control panel you can select thick lines.
**PARAMETER SWEEPS**

Sweep
VT0 = 0.5, 1.0, 2.0

W = 5u 20u 40u

TOX = 10n 20n 30n
3. UTMOST III Modeling Manual-Vol.1, Ch. 5, From Silvaco International.
7. ICCAP Manual, Hewlet Packard
8. PSpice Users Guide.
9. Dr. Fuller’s webpage: http://people.rit.edu/ffeee
Homework is due one week after this presentation was completed in class.

1. Do LTSPICE simulations for all the examples in this document.
2. Do an LTSPICE simulation for sub-CMOS 150 PMOS FET.