Introduction to the Long and Short Channel MOSFET

Dr. Lynn Fuller
Webpage: http://people.rit.edu/lffeee
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604

Email: Lynn.Fuller@rit.edu
Department webpage: http://www.rit.edu/kgcoe/microelectronic/
This PowerPoint module has been published using Adobe Presenter. Please click on the **Notes** tab in the left panel to read the instructors comments for each slide. Manually advance the slide by clicking on the **play** arrow or pressing the **page down** key.
OUTLINE

- Long Channel vs. Short Channel
- MOSFET I-V Characteristics
- MOS Threshold Voltage
- Lambda, Gamma, Kappa
- Leff
- VT Rolloff, DIBL
- Punchthrough
- Mobility, Effective Mobility, Theta, Vmax, Eta
- Gate Oxide Leakage
- Salacide
- Work Function Engineering, Surface/Buried Channel
- Strained Silicon, Current Drive in MOSFETs
- FIN FETS
- References
- Homework
Long-channel MOSFET is defined as devices with width and length long enough so that edge effects from the four sides can be neglected. Channel length L must be much greater than the sum of the drain and source depletion widths. The goal is to make tiny long channel devices.
LAMBDA, Lmin, Ldrawn, Lmask, Lpoly, Lint, Leff, L

- **Ldrawn** = what was drawn
- **Lmask** = ? Depends on +/-bias
- **Lpoly** after poly etch
- **Lpoly** after poly reoxidation
- **Lresist after photo** (resist trimming?)
- **L** = distance between space charge layers, when Vd= what it is

**Extracted Channel Length Parameters** = anything that makes the fit good (not real)

Source at 0 V

Drain at 3.3V

- Internally, Lint = distance between junctions, including under diffusion
- **Effective Channel Length**, Leff = distance between space charge layers, Vd = Vs = 0
- **Channel Length**, L, = distance between space charge layers, when Vd= what it is

- **Lambda** = design rule parameter, \( \lambda \), ie 0.25\( \mu \text{m} \)
- **Lmin** = min drawn poly length, \( 2\lambda \) 0.50\( \mu \text{m} \)
- **Ldrawn** = 0.35\( \mu \text{m} \)
- **Lmask** = 0.40\( \mu \text{m} \)
- **Lpoly** = 0.30\( \mu \text{m} \)
- **Lint** = 0.30\( \mu \text{m} \)
- **Leff** = 0.27\( \mu \text{m} \)
- **L** = 0.11\( \mu \text{m} \)
UNIFORMLY DOPED PN JUNCTION

**Space Charge Layer**

- Phosphorous donor atom and electron \( \text{P}^+ \)
- Ionized Immobile Phosphorous donor atom \( \text{P}^+ \)
- Ionized Immobile Boron acceptor atom \( \text{B}^- \)
- Boron acceptor atom and hole \( \text{B}^- \)

**Potential, \( \Psi \)**

\[ qN_A W_1 = qN_D W_2 \]

**Electric Field, \( \mathbf{\varepsilon} \)**

\[ \mathbf{\varepsilon}_0 \]

**Charge density, \( \rho \)**

\[ +qN_D \]

\[ -qN_A \]

\[ -W_1 \]

\[ W_2 \]

**Potentials**

\[ \Psi_0 + V_R \]
PROCESS CALCULATIONS

Built in Voltage:
\[ \Psi_0 = \frac{KT}{q} \ln \left( \frac{N_a N_d}{n_i^2} \right) \]

Width of Space Charge Layer:
\[ W_{sc} = \left[ \frac{2\varepsilon}{q}(\Psi_0 + V_R)(1/N_a + 1/N_d) \right]^{1/2} \]
\[ E_0 = - \left[ \frac{2q}{\varepsilon}(\Psi_0 + V_R) \frac{N_a N_d}{(N_a+N_d)} \right]^{1/2} \]

Example:
\[ \Psi_0 = 0.026 \ln \left( 1\times10^{17} 1\times10^{17}/1.45\times10^{10} \right) = 0.82 \]
\[ W_{sc @ 0V} = \left[ \frac{2(11.7)(8.85\times10^{-14})}{1.6\times10^{-19}}(0.82)(1/1\times10^{17} + 1/1\times10^{17}) \right]^{1/2} \]
\[ = 0.15 \mu m \text{ and } 0.07 \mu m \text{ on each side of the junction} \]
\[ W_{sc @ 3.3V} = \left[ \frac{2(11.7)(8.85\times10^{-14})}{1.6\times10^{-19}}(0.82+3.3)(1/1\times10^{17}) \right]^{1/2} \]
\[ = 0.33 \mu m \text{ and } 0.16 \mu m \text{ on each side of the junction} \]
\[ E_0 = - 2.5\times10^5 \text{ V/cm} \]

Source at 0 V \hspace{1cm} Drain at 3.3V

\[ \varepsilon = \varepsilon_0 \varepsilon_r = 8.85\times10^{-12} \ (11.7) \text{ F/m} \]

\[ \text{Leff} = 0.5 - 0.07 - 0.16 = \sim 0.27 \mu m \]
EXAMPLE CALCULATIONS

**CALCULATIONS FOR PN JUNCTION (ELECTROSTATICS)**

**Dr. Lynn Fuller**

To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

**CONSTANTS**

- \( K = 1.38 \times 10^{-23} \text{ J/K} \)
- \( q = 1.602 \times 10^{-19} \text{ C} \)
- \( E_0 = 1.12 \text{ eV} \)
- \( \varepsilon_0 = 8.85 \times 10^{-14} \text{ F/cm} \)
- \( c = 3.00 \times 10^8 \text{ cm/s} \)
- \( n_i = 1.45 \times 10^{10} \text{ cm}^{-3} \)
- \( N_D = 1.00 \times 10^{16} \text{ cm}^{-3} \)
- \( N_A = 5.00 \times 10^{11} \text{ cm}^{-3} \)
- \( V_r = 30 \text{ Volts} \)
- \( E_{\text{breakdown}} = 3.00 \times 10^5 \text{ V/cm} \)

**VARIABLES**

- \( T = 300 \text{ K} \)
- \( N_A = 5.00 \times 10^{11} \text{ cm}^{-3} \)
- \( N_D = 1.00 \times 10^{16} \text{ cm}^{-3} \)
- \( V_r = 30 \text{ Volts} \)

**CALCULATIONS:**

\[
E_g = E_0 - (eT^2/2)(T + 25)
\]

\[
E_g = 1.12 - (e(300^2/2)(300 + 25)) \quad \text{eV}
\]

\[
kT/q = 1.075 \text{ eV}
\]

\[
V_{bi} = (kT/q) \ln(N_A/N_D/n_i^2)
\]

\[
V_{bi} = (1.075/1.602 \times 10^{-19}) \ln(5.00 \times 10^{11}/1.00 \times 10^{16}/1.45 \times 10^{10})^2
\]

\[
V_{bi} = 0.76 \text{ Volts}
\]

\[
W = [(2q)/[(V_{bi} + V)N_A + N_D]]^{0.5}
\]

\[
W = [(2 \times 1.602 \times 10^{-19})/[(0.76 + V)5.00 \times 10^{11} + 1.00 \times 10^{16}]]^{0.5}
\]

\[
W = 2.02 \mu m
\]

\[
W = [V/(N_A + N_D)]^{0.5}
\]

\[
W = [V/(5.00 \times 10^{11} + 1.00 \times 10^{16})]^{0.5}
\]

\[
W = 0.04 \mu m
\]

\[
W = [V/(N_D/N_A)]^{0.5}
\]

\[
W = [V/(1.00 \times 10^{16}/5.00 \times 10^{11})]^{0.5}
\]

\[
W = 1.38 \mu m
\]

\[
E_{0} = -(q(V_{bi} + V)N_A/(N_A + N_D))^{0.5}
\]

\[
E_{0} = -(1.602 \times 10^{-19}(0.76 + V)5.00 \times 10^{11}/(5.00 \times 10^{11} + 1.00 \times 10^{16}))^{0.5}
\]

\[
E_{0} = -3.05 \times 10^5 \text{ V/cm}
\]

\[
C' = e\varepsilon_0 W
\]

\[
C' = (1.602 \times 10^{-19} \times 8.85 \times 10^{-14} \times 2.02 \mu m)
\]

\[
C' = 5.16 \times 10^{-9} \text{ F/cm}^2
\]

\[
\text{pn_electrostatics_current_temp.xls}
\]

\[
I_d = I_s(e^{q(V+KT)/kT} - 1)
\]

<table>
<thead>
<tr>
<th>( V )</th>
<th>( I_d )</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>-3.73E-13</td>
</tr>
<tr>
<td>-0.8</td>
<td>-3.73E-13</td>
</tr>
<tr>
<td>-0.7</td>
<td>-3.73E-13</td>
</tr>
<tr>
<td>-0.6</td>
<td>-3.73E-13</td>
</tr>
<tr>
<td>-0.5</td>
<td>-3.73E-13</td>
</tr>
<tr>
<td>-0.4</td>
<td>-3.73E-13</td>
</tr>
<tr>
<td>0.1</td>
<td>4.53E-11</td>
</tr>
<tr>
<td>0.2</td>
<td>2.20E-09</td>
</tr>
<tr>
<td>0.3</td>
<td>1.04E-07</td>
</tr>
<tr>
<td>0.4</td>
<td>4.39E-06</td>
</tr>
<tr>
<td>0.5</td>
<td>1.59E-05</td>
</tr>
<tr>
<td>0.6</td>
<td>5.74E-05</td>
</tr>
<tr>
<td>0.7</td>
<td>2.42E-05</td>
</tr>
<tr>
<td>0.8</td>
<td>9.46E-05</td>
</tr>
<tr>
<td>0.9</td>
<td>3.46E-05</td>
</tr>
<tr>
<td>1.0</td>
<td>1.00E-04</td>
</tr>
<tr>
<td>1.1</td>
<td>3.00E-04</td>
</tr>
<tr>
<td>1.2</td>
<td>9.00E-04</td>
</tr>
</tbody>
</table>

© February 3, 2019 Dr. Lynn Fuller, Professor
LONG CHANNEL NMOSFET I-V CHARACTERISTICS

Family of Curves

Saturation Region

Non Saturation Region

Saturation Region

Non Saturation Region

Subthreshold

Sub Vt Slope (mV/dec)

Subthreshold

Subthreshold
**LONG CHANNEL EQUATIONS FOR UO, VTO AND ID**

**Mobility:**

\[
\mu = \mu_{\text{min}} + \frac{(\mu_{\text{max}} - \mu_{\text{min}})}{\{1 + (N/N_{\text{ref}})\alpha\}}
\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Arsenic</th>
<th>Phosphorous</th>
<th>Boron</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\mu_{\text{min}})</td>
<td>52.2</td>
<td>68.5</td>
<td>44.9</td>
</tr>
<tr>
<td>(\mu_{\text{max}})</td>
<td>1417</td>
<td>1414</td>
<td>470.5</td>
</tr>
<tr>
<td>(N_{\text{ref}})</td>
<td>9.68X10^{16}</td>
<td>9.20X10^{16}</td>
<td>2.23X10^{17}</td>
</tr>
<tr>
<td>(\alpha)</td>
<td>0.680</td>
<td>0.711</td>
<td>0.719</td>
</tr>
</tbody>
</table>

**Threshold Voltage:**

\[V_{\text{TO}} = \Phi_m - q NSS/Cox' +/- 2[\Phi F] +/- 2 (q\varepsilon NSUB [\Phi F])^{0.5}/Cox'
\]

\[\Phi F = (KT/q) \ln (NSUB/ni)\]

where \(ni = 1.45E10\) and \(KT/q = 0.026\)

**Drain Current:**

- **Non-Saturation**

\[I_D = \mu W Cox' (V_g - V_t - V_d/2)V_d/L\]

- **Saturation**

\[I_{\text{Dsat}} = \mu W Cox' (V_g - V_t)^2/2L\]

\(Cox' = \varepsilon \varepsilon_0 / TOX = 3.9 \varepsilon_0 / TOX\)
LONG CHANNEL THRESHOLD VOLTAGE, VT

Flat-band Voltage  
\[ V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C'_{ox}} - \frac{1}{C'_{ox}} \int_0^{X_{ox}} \frac{X}{X_{ox}} \rho(x) \, dx \]

p-type substrate  
(n-channel)

Bulk Potential:  
\[ \phi_p = -kT/q \ln \left( \frac{N_A}{n_i} \right) \]

Work Function Difference  
\[ \phi_{MS} = \phi_M - (X + Eg/2q + [\phi_p]) \]

*Maximum Depletion Width:  
\[ \sqrt{\frac{4 \varepsilon_s [\phi_p]}{q N_a}} \]

NMOS Threshold Voltage:  
\[ VT = V_{FB} + 2[\phi_p] + \frac{1}{C'_{ox}} \sqrt{\frac{2 \varepsilon_s q N_a}{2[\phi_p]}} \]

p-type substrate

PMOS Threshold Voltage:  
\[ VT = V_{FB} - 2[\phi_n] - \frac{1}{C'_{ox}} \sqrt{\frac{2 \varepsilon_s q N_d}{2[\phi_n]}} \]

n-type substrate

Bulk Potential:  
\[ \phi_n = +kT/q \ln \left( \frac{N_D}{n_i} \right) \]

Work Function Difference  
\[ \phi_{MS} = \phi_M - (X + Eg/2q - [\phi_n]) \]

*Maximum Depletion Width:  
\[ \sqrt{\frac{4 \varepsilon_s [\phi_n]}{q N_d}} \]
DISCUSSION OF MOSFET VT EQUATIONS

These are the equations for MOSFET threshold voltage. The flat band voltage would be zero if the gate material and the semiconductor material had the same work function and the value of Qss (surface state density) was zero and no trapped charge in the oxide (Rho(x)) in the third term. The work function is a material property and in semiconductors also depends on the doping concentration. If the gate was n-type poly and the FET was p-type (n-well) and the doping of the n-type poly was equal to the doping at the surface of the n-well was the same then the Phi MS would be zero. Typically Phi MS is not zero. Qss is always positive because that charge comes from surface states created by the loss of electrons from some silicon atoms at the surface because silicon dioxide can not covalently bond with all the silicon atoms available and thus some electrons migrate away from the surface leaving a positive surface charge. The second term in the equation for threshold voltage is 2 Phi which is the semiconductor potential at threshold voltage where the surface is inverted to a concentration equal in magnitude to the concentration in the bulk. The last term is a voltage Q over C’ox that depends on the doping concentration at the surface, assuming source and substrate are at the same voltage. Similar to the semiconductor built-in voltage plus reverse bias voltage in a uniformly doped pn junction (~0.7 + VR). The body effect comes from this term.
Body Effect coefficient GAMMA or $\gamma$:

$$\gamma = \frac{1}{C_{ox} \varepsilon_{Si}} \sqrt{2q \varepsilon_{Si} N_{sub}}$$

$$V_T = \Phi_{MS} - \frac{Q_{ss}}{C_{ox}} + 2\phi_F + \gamma \sqrt{2\phi_F} + V_{SB}$$

where $\varepsilon_{Si} = 11.7$ and $\varepsilon_{ox} = 3.9$

$\varepsilon_0 = 8.8 \times 10^{-14}$ F/cm

$q = 1.6 \times 10^{-19}$
MAJOR FACTORS AFFECTING VTO

Gate work function, n+, p+, aluminum
Substrate doping, Nd or Na
Oxide thickness, Xox
Surface State Density, Nss or Qss

- n+ poly gate left scale
- p+ poly gate right scale
- Nss = 0
- Vbs = 0
- implant dose = zero

Nss is never zero, typically adds 0.5 volts
that is shifts both scales up 0.5 volts
APPROXIMATE LONG CHANNEL EQUATION FOR ID IN NON-SATURATION REGION

\[ I_D = \mu W Cox' (Vg-Vt-Vd/2)V_d \]

\[ Cox' = Cox/Area = \varepsilon_0\varepsilon_r/Xox \]
and Area = WL
and Xox is gate oxide thickness

Estimate \( I_D \) = charge in transit divided by the transit time

charge in transit \( Q = (Q \text{ source end } + Q \text{ drain end}) \) ave
\[ Q = CV = [Cox(Vg-Vs-Vt)+Cox(Vg-Vd-Vt)]/2 \]
\[ Q = Cox(Vg-Vt-Vd/2) = Cox'WL(Vg-Vt-Vd/2) \]

Transit time = distance/velocity = \( L/v = L/\mu E = L/\mu(Vd/L) = L^2/\mu Vd \)

\( E \) is electric field mobility
nMOSFET with $V_t=1$, since the Drain is at 0.1 volts and the source is at zero. Both drain and source will be on at gate voltages greater than 1.1 volt. The transistor will be in the non saturation region.
APPROXIMATE LONG CHANNEL EQUATION FOR ID IN SATURATION REGION

\[ I_{D_{\text{sat}}} = \mu W \frac{C_\text{ox'}}{2L} (V_{g} - V_{t})^2 \]

If \( V_d \) increases eventually \( V_g - V_d \) will be less than \( V_t \) and further increases in \( V_d \) will not cause increases in \( I_D \) (because the additional voltage will be across the gap region at the drain end where it can not reduce the transit time)

So substitute \( V_g - V_d = V_t \) or \( V_d = V_g - V_t \) into equation for non saturation region to get equation for saturation region.
SATURATION REGION CHARACTERISTICS

nMOSFET with Vt=1, Drain end is never on because Voltage Gate to Drain is Zero. Therefore this transistor is always in Saturation Region if the gate voltage is above the threshold voltage.
### MOSFET Long & Short Introduction

**CALCULATOR FOR IDEAL I-V CHARACTERISTICS**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
<th>M</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>14</td>
<td>15</td>
<td>16</td>
<td>17</td>
</tr>
<tr>
<td>CONSTANTS</td>
<td>VARIABLES</td>
<td>CHOOSE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T=</td>
<td>300 K</td>
<td>Na =</td>
<td>1.00E+18 cm⁻³</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>KT/q=</td>
<td>0.026 volts</td>
<td>Na⁺ Pol gate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ni=</td>
<td>1.45E+10 cm⁻³</td>
<td>N⁺ Pol gate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E₀=</td>
<td>8.852E⁻¹⁴ F/cm</td>
<td>N substr (pMOSFET)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Eₘ=</td>
<td>11.7</td>
<td>P substr (nMOSFET)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Er SiO₂=</td>
<td>3.9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tn=T/300=</td>
<td>1.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>q=</td>
<td>4.15 volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Eg=</td>
<td>1.124 volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.

**Mobility Calculations**

- Bulk mobility, \( U₀ = 450 \, \text{cm}²/\text{(V·sec)} \)
- Channel mobility, \( U_{eff} = 230 \, \text{cm}²/\text{(V·sec)} \)

**Threshold Voltage Calculations:**

- Metal Work Function: \( 4.12298855 \, \text{volts} \)
- Semiconductor Potential: \( 0.28967541 \, \text{volts} \)
- Oxide Capacitance/cm²: \( 6.903E-08 \, \text{F/cm²} \)
- Metal Semi Work Function Diff: \( -2.99E-01 \, \text{volts} \)
- Flat Band Voltage: \( -9.95E-01 \, \text{volts} \)
- Threshold Voltage: \( -1.7747834 \, \text{volts} \)

**IDS Calculations:**

- In Non Saturation Region: \( I_{ds} = \mu Cox' W/L (V_{gs}-V_t-V_{d})V_{d} \)
- In Saturation Region: \( I_{ds} = \mu Cox' W/2L (V_{gs} - V_t)^2 \)

**Gate Voltage Diagram**

- Source \( V_s \)
- Gate \( V_g \)
- Drain \( V_d \)

**L**

**References:**

- Kamins, Muller and Chang: 3rd Ed., 2003, pg 33
CALCULATOR FOR IDEAL $I$-$V$ CHARACTERISTICS

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
<th>M</th>
<th>N</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>41</td>
<td>Id @ Vgs =</td>
<td>Id @ Vgs</td>
<td>Id @ Vgs</td>
<td>Vds</td>
<td>4</td>
<td>6</td>
<td>8</td>
<td>10</td>
<td>Idsat</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>43</td>
<td>0.4</td>
<td>2.57E-05</td>
<td>5.1E-05</td>
<td>9E-05</td>
<td>0.00010188</td>
<td>2.5391E-05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>45</td>
<td>0.8</td>
<td>4.034E-03</td>
<td>9.7E-03</td>
<td>0.00019869</td>
<td>1.01354E-05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>47</td>
<td>1.2</td>
<td>6.19E-05</td>
<td>0.000142</td>
<td>0.00020942</td>
<td>2.28519E-05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>49</td>
<td>1.6</td>
<td>7.23E-05</td>
<td>0.00017</td>
<td>0.00037707</td>
<td>4.06256E-05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>51</td>
<td>2.0</td>
<td>7.78E-05</td>
<td>0.0002</td>
<td>0.00045864</td>
<td>6.34775E-05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>53</td>
<td>2.4</td>
<td>7.81E-05</td>
<td>0.00023</td>
<td>0.00053513</td>
<td>9.14076E-05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>55</td>
<td>2.8</td>
<td>7.33E-05</td>
<td>0.00025</td>
<td>0.00060655</td>
<td>0.000124415</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>57</td>
<td>3.2</td>
<td>6.35E-05</td>
<td>0.00027</td>
<td>0.00067289</td>
<td>0.000162302</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>59</td>
<td>3.6</td>
<td>4.85E-05</td>
<td>0.00028</td>
<td>0.00073413</td>
<td>0.000205667</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>61</td>
<td>4.0</td>
<td>2.86E-05</td>
<td>0.00028</td>
<td>0.00079033</td>
<td>0.00025391</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>63</td>
<td>4.4</td>
<td>3.52E-05</td>
<td>0.00028</td>
<td>0.00084145</td>
<td>0.000307231</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>65</td>
<td>4.8</td>
<td>2.62E-05</td>
<td>0.00028</td>
<td>0.00088745</td>
<td>0.00036563</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66</td>
<td>67</td>
<td>5.2</td>
<td>6.18E-05</td>
<td>0.00027</td>
<td>0.00092824</td>
<td>0.00042108</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>69</td>
<td>5.6</td>
<td>-0.0001022</td>
<td>0.00025</td>
<td>0.00096427</td>
<td>0.000497664</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>71</td>
<td>6.0</td>
<td>-0.0001475</td>
<td>0.00023</td>
<td>0.00099506</td>
<td>0.000571298</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>73</td>
<td>6.4</td>
<td>-0.000198</td>
<td>0.00021</td>
<td>0.00102077</td>
<td>0.00065001</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>75</td>
<td>6.8</td>
<td>-0.0002535</td>
<td>0.00018</td>
<td>0.0010414</td>
<td>0.0007333</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>76</td>
<td>77</td>
<td>7.2</td>
<td>-0.0003142</td>
<td>0.00014</td>
<td>0.0010596</td>
<td>0.000822668</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>78</td>
<td>79</td>
<td>7.6</td>
<td>-0.0003799</td>
<td>0.0001</td>
<td>0.00106743</td>
<td>0.000916615</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>81</td>
<td>8.0</td>
<td>-0.0004506</td>
<td>0.000</td>
<td>0.00107283</td>
<td>0.00101564</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>83</td>
<td>8.4</td>
<td>-0.0005263</td>
<td>0.000</td>
<td>0.00107313</td>
<td>0.00111974</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>85</td>
<td>8.8</td>
<td>-0.0006074</td>
<td>0.000</td>
<td>0.0010684</td>
<td>0.001225924</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>86</td>
<td>87</td>
<td>9.2</td>
<td>-0.0006934</td>
<td>0.000</td>
<td>0.00105856</td>
<td>0.00134184</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>88</td>
<td>89</td>
<td>9.6</td>
<td>-0.0007845</td>
<td>0.000</td>
<td>0.00104365</td>
<td>0.00146522</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td>91</td>
<td>10.0</td>
<td>-0.0008807</td>
<td>0.000</td>
<td>0.00102365</td>
<td>0.00158693</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: for NMOS $I_d$, $V_d$, $V_{gs}$ are all positive for PMOS $I_d$, $V_d$, $V_{gs}$ are all negative but are shown as positive.
The Short Channel MOSFET

Sort channel MOSFET is defined as devices with width and length short enough such that the edge effects cannot be neglected.

Channel length $L_{eff}$ is comparable to the depletion widths associated with the drain and source.
Terada-Muta Method for Leff and Rds

In the linear region ($V_D$ is small):

$$I_D = \frac{\mu W \text{ Cox}' (V_{gs} - V_t - V_d/2)}{V_D} V_D$$

Leff = Lm - $\Delta$L

where $\Delta$L is correction due to processing

Lm is the mask length

$$R_m = \frac{V_D}{I_D} = \text{measured resistance}$$

= $R_{ds} + (Lm - \Delta L)/ \mu W \text{ Cox}' (V_{gs} - V_t)$

so measure $R_m$ for different channel length transistors and plot $R_m$ vs Lm

where $R_m = \text{intersect find value for } \Delta L \text{ and } R_{ds}$

Then Leff can be calculated for each different length transistor from

Leff = Lm - $\Delta$L
Linear Region:

\[ V_D = 0.1V \]
\[ V_G - V_T \gg I_D R_{SD} \]

At low \( I_D \), \( V_{RSD} \) small

\[
R_m = \frac{V_d}{I_d} = R_{SD} + \frac{(L_{mask} - \Delta L)}{\mu C_{ox} W (V_{GS} - V_t)}
\]

\( L_{eff} = L_{mask} - \Delta L \)
\( L_{eff} = 0.5 \mu m - 0.3 \mu m \)
\( L_{eff} = 0.2 \mu m \)

Plot \( R_m \) vs. \( L_{mask} \) for different \( V_{GS} - V_t \)
**CHANNEL LENGTH MODULATION - LAMBDA**

Channel Length Modulation
Parameter $\lambda$

$\lambda = \text{Slope} / \text{Idsat}$

Non-Saturation Region

\[ I_{D_{\text{sat}}} = \frac{\mu W \text{Cox'} (V_{g} - V_{t})^{2} (1 + \lambda V_{d}s)}{2L} \]

Saturation Region

\[ I_{D} = \frac{\mu W \text{Cox'} (V_{g} - V_{t} - V_{d}/2)V_{d} (1 + \lambda V_{d}s)}{L} \]

Note: $\lambda$ is different for each different channel length, L.
KAPPA is channel length modulation parameter.

KAPPA is calculated:

\[ Kappa = \left( \frac{qN_{sub}/(2\varepsilon_o\varepsilon_r)(1-Ids'/Id')(L-2LD-Xdso-Xds)^2)}{(Vd2-Vdsat)} \right)^{0.5} \]

Measure \( Id' \) at large \( Vds \), and \( Id_{sat} \) at \( Vdsat \),
Kappa has units of 1/V, typical value \(~0.1\)

Note: Kappa is not different for each different channel length, \( L \),
Kappa combined with other parameters determine the slope in saturation.
As the channel length decreases, the channel depletion region becomes smaller and $V_{GS}$ needed to turn on the channel appears to decrease, that is $VT$ appears to decrease.

A similar effect occurs for increasing $V_{DS}$ which causes an increase in the drain space charge layer. Called Drain Induced Barrier Lowering or DIBL.
A Test Chip is used that includes nMOS and pMOS transistors of various lengths from 0.1 µm to 5.0 µm and the threshold voltage is plotted versus channel length. The threshold voltage needs to be high enough so that when the input is zero or +Vsupply the transistor current is many decades lower than when it is on. Vt and sub-Vt slope interact.
NARROW GATE WIDTH EFFECTS

Fringing field causes channel depletion region to extend beyond the gate in the width direction. Thus additional gate charge is required causing an apparent increase in threshold voltage. In wide channel devices this can be neglected but as the channel becomes smaller it is more important.

In NMOS devices encroachment of the channel stop impurity atoms under the gate edges causing the edges to be heavier doped requiring more charge on the gate to turn on the entire channel width. In PMOSFETs the phosphorous pile up at the surface under the field region causes a similar apparent increase in doping at the edges of the channel width.
VT initially increases with decrease in channel length then decreases. This is caused by various effects that result in lateral dopant nonuniformity in the channel.

Example: Oxidation Enhanced Diffusion or enhanced diffusion due to implant damage causing the dopant concentration to be higher in the channel near the drain and source edges of the poly gate.
DELTA is introduced to model narrow channel effects on threshold voltage. The parameter WD (channel width reduction from drawn value) is used to calculate the effective channel width. DELTA is used in the calculation of threshold voltage.

$$\Delta = \frac{q \, N_{SUB} \, X_{ds}^2}{\varepsilon_0 \, \varepsilon_i \, 2 \, \Phi}$$

Note: a dimensionless number typically ~3
The subthreshold characteristics are important in VLSI circuits because when the transistors are off they should not carry much current since there are so many transistors. (subthreshold slope typical value about 100 mV/decade, theoretical maximum of 63mV/dec at room T). Thinner gate oxide makes subthreshold slope larger. Surface channel has larger slope than buried channel. Larger slope is better.
DRAIN INDUCED BARRIER LOWERING

DIBL = change in VG /change in VD at ID=1E-9 amps/µm or 1.6E-8 amps for this size transistor

= ~ (1.19-1.14)/(5-0.1) = ~ 10mV/V

L/W=2/16
The parameter ETA is used to describe DIBL (Drain Induced Barrier Lowering) resulting in a modification to the LEVEL 1 equation for threshold voltage.

\[ V_{TO} = \Phi_{ms} - \phi_{\text{ETA}} - q \frac{\text{NSS}}{C_{ox'}} - 2 \Phi k - 2 (q\varepsilon s \text{NSUB } \Phi F)^{0.5}/C_{ox'} \]

\[ \phi_{\text{ETA}} = \frac{(-8.14E-22)\times\text{ETA}}{C_{ox'\text{Leff}}^{3}} \times V_{ds} \]
As the voltage on the drain increases the space charge associated with the drain pn junction increases. Current flow through the transistor increases as the source and drain space charge layers approach each other. This is called **punchthrough**. The first indication is an increase in the subthreshold current and a decrease in the subthreshold slope.
**PUNCHTHROUGH**

Long channel behavior

Short channel behavior

**Punchthrough**
MEASURED ID-VDS FAMILY SHOWING PUNCHTHROUGH

Punchthrough
Punch through implant increases the well doping below the drain and source depth making the space charge layer smaller.
PUNCHTHROUGH HALO IMPLANT

Boron Implant at High Angle

Gate

Source

Drain

P-type well
Well Profiles (a)

Fig. 1. SIMS measurement of the channel implant for nMOS and pMOS (a), and the source-drain extension/halo profiles for nMOS (b) and pMOS (c).
WHY THE D/S NEEDS TO BE SHALLOW

Sketch the three space charge layers
- The Channel Space Charge
- The Drain Space Charge
- The Source Space Charge

Look at Punchthrough

Punchthrough will occur at lower drain voltages in the device with deeper D/S
\[ I_D = \mu W \frac{Cox'}{(V_g - V_t - V_d/2)V_d}{L} \]

Non Saturation Region

\[ I_{D_{\text{sat}}} = \frac{\mu W Cox'}{2L} (V_g - V_t)^2 \]

Saturation Region

Mobility (\(\mu\)) decreases with increase in doping concentration (and many other things)
Electron and hole mobilities in silicon at 300 K as functions of the total dopant concentration (N). The values plotted are the results of the curve fitting measurements from several sources. The mobility curves can be generated using the equation below with the parameters shown:

\[
\mu(N) = \mu_{\text{min}} + \frac{\mu_{\text{max}} - \mu_{\text{min}}}{1 + (N/N_{\text{ref}})^{\alpha}}
\]

- **Parameter** | **Arsenic** | **Phosphorous** | **Boron**
- \(\mu_{\text{min}}\) | 52.2 | 68.5 | 44.9
- \(\mu_{\text{max}}\) | 1417 | 1414 | 470.5
- \(N_{\text{ref}}\) | 9.68X10^{16} | 9.20X10^{16} | 2.23X10^{17}
- \(\alpha\) | 0.680 | 0.711 | 0.719

From Muller and Kamins, 3rd Ed., pg 33
In a MOSFET the mobility is lower than the bulk mobility because of the scattering with the Si-SiO2 interface. The vertical electric field causes the carriers to keep bumping into the interface causing the mobility to degrade. The electric fields can be $1E5$ or $1E6$ V/cm and at that level the collisions with the interface reduce the mobility even more. The vertical electrical field is higher for heavier doped substrates and when Vt adjust implants are used.
MOBILITY DEGRADATION

short channel

long channel

Note: Id should follow green line in long channel devices
The mobility used in the equations for $I_{ds}$ is the effective mobility, $U_{eff}$. Starting with $U_{O}$ from level 1, $U_{eff}$ is found. The parameter THETA is introduced to model mobility degradation due to high vertical electric fields (larger values of $V_{gs} - V_{TO}$).

$$U_{eff}^* = \frac{U_{O}}{(1+\text{THETA} \ (V_{gs} - V_{TO}))}$$

Measure $I_{ds}$ for a wide transistor with low value of $V_{ds}$ and large value of $V_{gs}$ and using $L_{eff}$ from Terata-Muta method and $\lambda$ from level 1, calculate THETA from these two equations.

$$I_{dsat} = \frac{U_{eff} \ W \ Cox' \ (V_{g} - V_{t})^2 \ (1 + \lambda V_{ds})}{2L_{eff}}$$

Warning: Curvature also due to $R_{DS}$ so $V_{ds}$ is $(V_{applied} - R_{ds}*I_{dsat})$ requires an iterative approach to find THETA.
Carriers in semiconductors typically move in response to an applied electric field. The carrier velocity is proportional to the applied electric field. The proportionality constant is the mobility.

Velocity = mobility x electric field = \( \mu E \)

At very high electric fields this relationship ceases to be accurate. The carrier velocity stops increasing (or we say saturates). In a one micrometer channel length device with one volt across it, the electric field is 1E4 V/cm.

Velocity (cm/sec) vs E (V/cm)
VELOCITY SATURATION

Note: $I_d$ should increase with $(V_{gs} - V_{t})^2$ in long channel devices.
The parameter $V_{MAX}$ is introduced to model the decrease in mobility at higher $V_{ds}$ due to velocity saturation. Ideally, carrier velocity is directly proportional to the applied electric field. However, at very high lateral electric fields, $E_x$, this relationship ceases to be accurate - the carrier velocity saturates at $V_{MAX}$.

$$U_{eff} = \frac{U_O}{1 + U_O \frac{v_{de}}{V_{MAX} L_{eff}}}$$

Where, $V_{de} = \min (V_{ds}, V_{dsat})$

Note: other models (equations) for mobility exist and use parameters such as $UCRIT$, $UEXP$, $ULTRA$, $ECRIT$, $ESAT$
LOW DOPED DRAIN REDUCES LATERAL FIELD

- Low Doped Drain
- Side wall Spacer
- Silicide
- Gate
- Source
- Drain
- Field Oxide
- Stop
- P-type Punch Through Implant
- P-type well
The gate should be as thin as possible to reduce the short channel effects. In addition there is a limit imposed by considerations that affect the long term reliability of the gate oxide. This requirement imposes a maximum allowed electric field in the oxide under the long term normal operating conditions. This limit is chosen as 80% of the oxide field value at the on-set of Fowler-Nordheim (F-N) tunneling through the oxide. Since the latter is 5 MV/cm, a 4 MV/cm oxide field is considered as the maximum allowed for long term, reliable operation. For example:

For 2.5 volt operation, $X_{ox}$ is set at: $X_{ox} = \frac{V_{dd}}{E_{max}}$

$= \frac{2.5 \text{ V}}{4 \text{ MV/cm}} = 65 \text{ Å}$
Ti Salicide will reduce the sheet resistance of the poly and the drain and source regions. Salicide is an acronym for Self Aligned Silicide and Silicide is a material that is a combination of silicon and metal such as Ti, W or Co. These materials are formed by depositing a thin film of the metal on the wafer and then heating to form a Silicide. The Silicide forms only where the metal is in contact with the Silicon or poly. Etchants can remove the metal and leave the Silicide thus the term Self Aligned Silicide or SALICIDE.
**NMOS WITH N+ POLY GATE**

- Vt is typically negative or if positive near zero.
- Vt Adjust Implant is Boron in a P-type substrate making the NMOS transistor a surface channel device.

![Graph showing Boron Vt implant with depth into wafer (µm) and doping concentration (N_A cm^-3)]
PMOS WITH N+ POLY GATE

- Vt Can Not Be Positive Because All The Contributors To The Vt Are Negative. Even Making Qss=0 And Nd = Zero Does Not Make Vt Positive
- Vt Is Typically More Negative Than Desired Like -2 Volts
- Vt Adjust Implant Is Boron In An N-type Substrate Making The Pmos Transistor A Buried Channel Device (Charge Carriers Move Between Drain And Source At Some Distance Away From The Gate Oxide/Silicon Interface)
**PMOS WITH N+ POLY GATE**

- **N (cm^-3)**
  - 1E16

**Boron Vt Implant**

**Phosphorous n-type wafer**

**Depth into Wafer, µm**

- 0.0
- 0.2
- 0.4
- 0.6
Changes Work Function Of The Metal

Thus Metal-semiconductor Workfunction Difference Becomes About +1 Volt Rather Than ~0 Volts.

This Makes Vt More Positive Than Desired So An Ion Implant Of N-type Impurity Is Needed Making The Device A Surface Channel Device Rather Than A Buried Channel Device.
PMOS WITH P+ POLY GATE

![Graph showing Phosphorous Vt Implant]

- **N_D (cm⁻³):** 1E16
- **Depth into Wafer, µm:** 0.0, 0.2, 0.4, 0.6
- **Phosphorous n-type wafer**

**Phosphorous Vt Implant**

Rochester Institute of Technology
Microelectronic Engineering

© February 3, 2019 Dr. Lynn Fuller, Professor
SURFACE CHANNEL VS BURIED CHANNEL

- Surface Channel Devices Exhibit Higher Subthreshold Slope
- Surface Channel Devices Are Less Sensitive To Punch Through
- Surface Channel Devices Have Less Severe Threshold Voltage Rolloff
- Surface Channel Devices Have Higher Transconductance
- Surface Channel Devices Have About 15% Lower Carrier Mobility
Strained silicon can increase carrier mobility.
A simple way to think about strained silicon follows: Tensile strain causes the silicon atoms to be pulled further apart making it easier for electrons to move through the silicon. On the other hand moving the atoms further apart makes it harder for holes to move because holes require bound electrons to move from a silicon atom to a neighboring silicon atom in the opposite direction, which is more difficult if they are further apart. Thus tensile strain increases mobility in n-type silicon and compressive strain increases mobility in p-type silicon (devices).

Strain can be created globally or locally. Growing an epitaxial layer of silicon on a silicon/germanium substrate creates (global) biaxial tensile strain in the silicon. N-MOSFETS built on these wafers will have higher mobility. P-MOSFETS will have lower mobility. Local strain can be created for each transistor such that N-MOSFETS see tensile strain and P-MOSFETS see compressive strain improving both transistors mobility. Local strain techniques include capping layers and introducing Ge or C in the source/drain regions.
Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon–Carbon Source/Drain and Tensile-Stress Liner

Kah-Wee Ang, King-Jien Chui, Chih-Hang Tung, N. Balasubramanian, Ming-Fu Li, Ganesh S. Samudra, and Yee-Chia Yeo

Abstract—We report the demonstration of 25-nm gate-length $L_G$ strained nMOSFETs featuring the silicon–carbon source and drain ($Si_{1-y}C_y$ S/D) regions and a thin-body thickness $T_{body}$ of $\sim$18 nm. This is also the smallest reported planar nMOSFET with the $Si_{1-y}C_y$ S/D stressors. Strain-induced mobility enhancement due to the $Si_{1-y}C_y$ S/D leads to a significant drive-current $I_{Dsat}$ enhancement of 52% over the control transistor. Furthermore, the integration of tensile-stress SIN etch stop layer and $Si_{1-y}C_y$ S/D extends the $I_{Dsat}$ enhancement to 67%. The performance enhancement was achieved for the devices with similar subthreshold swing and drain-induced barrier lowering. The $Si_{1-y}C_y$ technology and its combination with the existing strained-silicon techniques are promising for the future high-performance CMOS applications.

Index Terms—Electron mobility, nMOSFET, silicon–carbon ($Si_{1-y}C_y$), silicon nitride liner, strain, stress.

I. INTRODUCTION

RECENTLY, channel-strain engineering is being actively pursued to enhance carrier mobility and drive current

Fig. 1. (a) SEM image showing problems of silicon migration during the high temperature (800 °C) prebake step in the $Si_{1-y}C_y$ selective epitaxy process. (b) Excellent morphology of $Si_{1-y}C_y$ on the S/D regions is demonstrated when a reduced prebake temperature (700 °C) and a tightly controlled SOI body thickness are used. (c) TEM micrograph of a strained n-channel transistor with the $Si_{1-y}C_y$ S/D stressors and the high stress ESL. This transistor features the physical gate length $L_G$ of 25 nm and the body thickness $T_{body}$ of $\sim$15 nm. A 25-nm-thick SIN ESL with the tensile stress of 1.1 GPa was used.
0.025µm STRAINED SILICON MOSFET

Fig. 2. (a) $I_{DS}-V_{DS}$ characteristics of the control and strained nMOSFETs with single stressor ($Si_{1-y}C_yS/D$) and dual stressors ($Si_{1-y}C_yS/D$ and tensile-stress SiN ESL). Significant $I_{Dsat}$ enhancement of 52% is observed in the single stressor device over the control transistor. Even higher $I_{Dsat}$ improvement of 67% is achieved with the integration of high stress ESL and $Si_{1-y}C_yS/D$. (b) Single and dual stressor strained devices are observed to enhance the transconductance by 95% and 139% over the control transistor, respectively.

Microelectronic Engineering
IV. CONCLUSION

We demonstrated the successful integration of the $\text{Si}_{1-y}\text{C}_y$ S/D regions in the strained SOI nMOSFETs with the 25-nm gate lengths, enhancing the $I_{D\text{sat}}$ by 52%. Excellent subthreshold characteristics are achieved by the aggressive scaling of the SOI body thickness. Strain effects and $I_{D\text{sat}}$ are enhanced further by combining the high stress ESL and the $\text{Si}_{1-y}\text{C}_y$ S/D stressors. Further performance boost can be achieved with an increased $\text{Si}_{1-y}\text{C}_y$ S/D elevation.
Partially Depleted silicon on Insulator
doped channel
100 nm or thicker silicon layer
floating body considerations

Thinner Si Epi Layer
Fully Depleted silicon on Insulator
undoped or lightly doped channel
50 nm or thinner silicon layer
TRIPLE GATE TRANSISTOR

- The drive currents are 446 uA/um for n-FinFET and 356 uA/um for p-FinFET respectively.
- The peak transconductance of the p-FinFET is very high (633uS/um at 105 nm $L_g$), because the hole mobility in the (110) channel is enhanced.
- Gate Delay is 0.34 ps for n-FET and 0.43 ps for p-FET respectively at 10 nm $L_g$.
- The subthreshold slope is ~60 mV/dec for n-FET and 101 mV/dec for p-FET respectively.
- The DIBL is 71 mV/V n-FET and 120 mV/V for p-FET respectively.

Qin Zhang, 04/19/2005
FIN FET

from: Arabinda Das and Alexandre Dorofeev, UBM Tech Insights
SUMMARY FOR FINFETS AND TRIPLE GATE FETS

1. Fin FETS have higher gm and Idrive because mobility is increased with lower doped channels.
2. Fin FETs have higher sub-threshold slope.
3. Fin FETS have lower DIBL
**FIN FETS IN FLASH MEMORY**

*FinFETs Used in Smallest Non-Volatile Flash Memory*

Peter Singer, Editor-In-Chief – 2/1/2005
Semiconductor International

Scientists at Infineon Technologies AG (Munich, Germany) have built the world's smallest non-volatile flash memory cell using finFETs. With gate dimensions measuring only 20 nm, the new memory cell would make non-volatile memory chips with a capacity of 32 Gb possible within a few years. That is 8× the capacity of what is currently available on the market.

Non-volatile flash memories are becoming increasingly popular as mass storage media for devices such as digital cameras, camcorders and USB sticks. The most advanced non-volatile flash memory devices available today can permanently store one or two bits of information per memory cell without a supply voltage.

The International Technology Roadmap for Semiconductors (ITRS) notes that future high-density flash memories for standalone data storage applications require devices with minimum feature size F smaller than 50 nm. To achieve that, Infineon researchers used a three-dimensional transistor device called the finFET, so named because part of the structure sticks up like a shark's fin. By wrapping the gate electrode around the gate dielectric, this type of device provides greater control over carrier flow and leakage current. When used in memory

20 nm gate length fin FETS used in worlds smallest flash memory cell.

Possible future chips with capacity of 32 Gbit.
SUMMARY

Today's most advanced devices have gate lengths near 10nm. Although the goal is to have long channel behavior it is difficult to achieve. There are many factors to consider and no simple solution. The models for simulation (SPICE) have become very complex.
REFERENCES

HOMEWORK – MOSFET

1. Calculate the IDS-VDS characteristics for a PMOS transistor for 0<VDS<5 built with the following parameters: substrate doping ND = 1E15 cm-3, Xox = 500 Å, N+ poly gate, Nss = 3E11, W = 32 µm, L = 16 µm

2. Use SPICE to simulate the IDS-VDS characteristics for the PMOS transistor above. Compare SPICE versus hand calculated (Excel).

3. Use SPICE to simulate the IDS-VDS characteristics for a NMOS transistor using a SPICE MOSFET model for L = 1um and for L = 0.1um. Let W be 10 times L.