PMOS Testing at Rochester Institute of Technology

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OUTLINE

- Test Chip
- Test Equipment
- Resistive Structures
- Transistors
- Integrated Circuits
- Ring Oscillator
- Digital Circuits

Shortcourse: Chip Size = 7mm x 7mm
20 rows and 21 columns
THE TEST CHIP

- Alignment Marks
- CD Linewidth, Overlay
- Van Der Pauw, p+ DS, Metal
- MOSFET’s,
- Inverters
- Ring Oscillator
- CBKR
- Digital Circuits
TEST FACILITY

- HP4145 Semiconductor Parameter Analyzer
- Keithley 7001 Switch Matrix
- Computer
- ICS Software
- Camera
- Ultracision Semi-Automatic Wafer Prober
- Test Fixture and Manual Probe Station
TEST EQUIPMENT

Automatic Prober

Semi-automatic Prober
TEST EQUIPMENT

Manual Prober
RESISTOR TEST RESULTS

\[ R = \frac{V}{I} = \frac{1}{\text{slope}} \]

\[ R = \frac{\text{Rhos}}{L/W} \]

\[ L/W = 400/60 \]

\[ R = 647 \, \Omega \]
VAN DER PAUW TEST STRUCTURES FOR SHEET RESISTANCE

\[ Rs = \frac{(V1-V2)}{I} \frac{\Pi}{\ln 2} \]
VAN DER PAUW TEST RESULTS

26.4 Ohms
CBKR AND INVERTERS
CROSS BRIDGE KELVIN RESISTANCE TEST STRUCTURES FOR CONTACT RESISTANCES

\[
R_c = \frac{(V_1 - V_2)}{I} \quad \text{ohms}
\]

\[
G_c = \frac{I}{(V_1 - V_2)} \cdot \frac{1}{W_1 \times W_2} \quad \text{mhos/µm}^2
\]
METAL AND DIFFUSION SERPENTINE

Defect density (in #/cm²) = (# defective x 1612) / (# tested)

Line width = 15 µm
Line Space = 30 µm
L/W = 269
Area Covered by metal = 62050 µm²

R = Rhos L/W
PMOS TRANSISTORS

Layout

Photograph

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PMOS TRANSISTOR TEST RESULTS

Tue EMCR 701 PMOSFET W=100um L=20um

Conditions:
Swp: SMU1
Start: 0.0000 V
Stop: -15.0000 V
Step: -0.1500 V
Pts: 101

Step: SMU2
Start: 0.0000 V
Stop: -14.0000 V
Step: -2.0000 V
Pts: 8

Con: SMU3
Val: 0.0000 V

Fit #1: None
Fit #2: None

<table>
<thead>
<tr>
<th>Cursors</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-15.0000</td>
<td>-4.7116m</td>
</tr>
<tr>
<td></td>
<td>-12.3000</td>
<td>-4.5924m</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11:47:42</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11/09/2010</td>
<td></td>
</tr>
</tbody>
</table>
PMOSFET with $V_t=-1$, since the Drain is at -0.1 volts and the source is at zero. Both drain and source will be on at gate voltages greater than -1.1 volt. The transistor will be in the non-saturation region.
LINEAR REGION TEST RESULTS

PMOSFET ID vs VGS

Conditions:
- Con: SMU1
- Val: -0.1000 V
- Swp: SMU2
- Start: -0.0100 V
- Stop: -5.0000 V
- Step: -0.0400 V
- Pts: 101
- Con: SMU3
- Val: 0.0000 V
- Con: SMU4
- Val: 0.0000 V

<table>
<thead>
<tr>
<th>Fit #1:</th>
<th>Fit #2:</th>
<th>Cursors: X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type: Linear</td>
<td>None</td>
<td>-1.7382</td>
<td>-2.5630u</td>
</tr>
<tr>
<td>Slp:8.2009u</td>
<td></td>
<td>-2.1345</td>
<td>-6.1845u</td>
</tr>
<tr>
<td>Y-Int:0.0134</td>
<td></td>
<td>-1.7886</td>
<td>-8.4017u</td>
</tr>
<tr>
<td>X-Int:-1.4559</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TRANSISTOR SATURATION REGION VT, GM

PMOS

\[ V_{gs} = V_{ds} \]

\[ I_d + \frac{V_{sub}}{V_{to}} \]

pMOSFET with \( V_t = -1 \), Drain end is never on because Voltage Gate to Drain is Zero. Therefore this transistor is always in Saturation Region if the gate voltage is above the threshold voltage.

\[ g_m = \Delta I_d / \Delta V_g \]
The subthreshold characteristics are important in VLSI circuits because when the transistors are off they should not carry much current since there are so many transistors. (typical value about 100 mV/decade)
INVERTERS

L = 40µm
W = 20µm
L = 20µm
W = 50µm
**INVERTERS**

Vin -> Vout

Inverter Gain = \( \sqrt{\frac{Wd/Ld}{Wu/Lu}} \)

Δ 0 noise margin = ViL - Voh

Δ 1 noise margin = Voh - Vih

PMOS Inverter with Enhancement Load

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INVERTER TEST RESULTS

Gain = -2.64

Conditions:
Con: SMU3
Val: -15.0000 V
Swp: SMU1
Start: 0.0000 V
Stop: -15.0000 V
Step: -0.1500 V
Pts: 101
Con: SMU4
Val: 0.0000 V
Con: SMU2
Val: 0.0000 A

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11/09/2010
RING OSCILLATOR, $td$

Seven stage ring oscillator with two output buffers

$td = T / 2 \times N$

$td = \text{gate delay}$

$N = \text{number of stages}$

$T = \text{period of oscillation}$

$V_{out}$

$T = \text{period of oscillation}$
9 STAGE RING OSCILLATOR
RING OSCILLATOR OUTPUT

\[ td = \frac{T}{2n} \]
\[ = \frac{500 \text{ ns}}{2 / 9} \]
\[ = 28 \text{ ns} \]
DIGITAL CIRCUIT TESTING

![Digital Circuit Diagram]
LAB VIEW SOFTWARE

Signal Input from Digital Circuit on a wafer

Input Signal Board

Output Signal Board

Signal Output to Digital Circuit on a wafer
HARDWARE FOR OUTPUT

6 Analog Outputs
Ribbon Cable
Terminal Board

AT-A0-6

- Available for ISA computers
- 6 analog outputs; 12-bit resolution, 300 kSPs maximum update rate
- 8 digital I/O lines (5 V TTL)
- 4.20 mA current sinks
- NI-DAQ driver with DAQ channel wizard for reduced configuration

NB1

- 50-pin ribbon cable for any board with a 50 pin connector
- Connects to 50pin connector accessories
- 1 m and 2 m length options
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information

CB50

- Low-cost accessory with 50 screw terminals for easily connecting field I/O signals to your DAQ board
- One 50-pin header for directly connecting to 50-pin cables
- Mounts on a standard DIN rail or flush on a wall or panel
- Dimensions: 13.5 by 7.3 cm (6.3 by 2.9 in)
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information
HARDWARE FOR INPUT

16 Analog Inputs
Ribbon Cable
Terminal Board

AT-MIO-16E-10

- Available for ISA computers
- Up to 16 analog inputs; 12-bit resolution; 100 kS/s sampling rate
- Two 12-bit analog outputs; 8 digital I/O lines; two 24-bit counters
- Calibration certificate included for NIST traceability
- NI-DAQ driver with DAQ channel wizard for reduced configuration

R6968

- 68-pin flat ribbon cable terminated with two 68-pin connectors
- 1 m length available
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information

TBX-68

- Termination accessory with 68 screw terminals
- Easy connection of field I/O signals to 68-pin DAQ devices
- Mounted in plastic base; includes hardware for mounting on a standard DIN rail
- Dimensions: 12.80 by 10.74 cm (4.92 by 4.23 in.)
- Download PDFs for compatibility charts, more detailed descriptions, and ordering information
FINAL SYSTEM

[Image of a laboratory setup with a computer, microscope, and test equipment.]

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Click on digital testing icon to invoke the lab view software and this main menu.

Click to select the type of test you wish to run.
NOR GATE AND NOR FLIP FLOP

PMOS 2 INPUT NOR

PMOS NOR RS Flip Flop

Figure 7 DIGITAL DEVICES
TESTING TWO INPUT ONE OUTPUT LOGIC GATES
FOUR CHOICES FOR SUPPLY VOLTAGES

CLICK TO SELECT ONE

- PMOS, \( V_{cc} = -10 \) Volts
- CMOS/TTL \( V_{cc} = +5 \) Volts
- NMOS, \( V_{cc} = +10 \) Volts
- ANALOG, \( V_{cc} = +5 \) Volts, \( V_{dd} = -5 \) Volts
PROBE CARD/WIRE CONNECTIONS
SWITCH MATRIX (MANUAL)

Supply
Vcc - V Gnd

Outputs
a b c d e f

Inputs
a b c d e f

Wire #17

Wire #8
RUN TEST

Click to Start Test
Stop Test

Click to Select
When
Output is
High or
Low

Test Results
For Xor Gate
PMOS INVERTER GAIN = 4
Test for PMOS Two Input NOR, Gain = 4 or 8
PMOS 2-INPUT XOR

PMOS Testing at RIT
nmos Vt target +1
0000000000000000
0000050505050000
0000000000000000
0050605070507000
0000000000000000
0040403040303000
0000000000000000
0040404040404000
0000000000000000
0040504050906000
0000000000000000
0050506060607000
0000000000000000
0000505050500000
0000000000000000

row 1 is the first row in which a full die is located
column 1 is the first column in which a full die is located
### WAFER MAPS FOR MESA

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>no die</td>
</tr>
<tr>
<td>1</td>
<td>value &lt; (Target - 40%)</td>
</tr>
<tr>
<td>2</td>
<td>(Target - 40%) &lt; value &lt; (Target - 30%)</td>
</tr>
<tr>
<td>3</td>
<td>(Target - 30%) &lt; value &lt; (Target - 20%)</td>
</tr>
<tr>
<td>4</td>
<td>(Target - 20%) &lt; value &lt; (Target - 10%)</td>
</tr>
<tr>
<td>5</td>
<td>(Target - 10%) &lt; value &lt; (Target + 10%)</td>
</tr>
<tr>
<td>6</td>
<td>(Target + 10%) &lt; value &lt; (Target + 20%)</td>
</tr>
<tr>
<td>7</td>
<td>(Target + 20%) &lt; value &lt; (Target + 30%)</td>
</tr>
<tr>
<td>8</td>
<td>(Target + 30%) &lt; value &lt; (Target + 40%)</td>
</tr>
<tr>
<td>9</td>
<td>(Target + 40%) &lt; value</td>
</tr>
</tbody>
</table>
Example: Given a wafer with test chips located as shown and nmos threshold voltage data encoded and stored in MESA as shown. Reconstruct a wafer map using EXCELL spreadsheet.
FUTURE WORK

- More Automation
- Improved Wafer Mapping
- More Complete Testing
CONCLUSION

- A test specification has been developed
- A history data base has been developed
- Testing is very time consuming. It takes us 9 hours to do all the specified tests and even then we only test a few devices on a wafer.
- Currently we test about 1% of the devices
REFERENCES

REVIEW QUESTIONS - PMOS TEST SPECIFICATION

1. How is Vt and gm found from the transistor family of curves.
2. Is the Vt and gm the same in the non-saturation region as in the saturation region?
3. What is the significance of the sub-threshold slope. What is the difference between sub-threshold slope and sub-threshold swing?
4. What is the significance of the noise margin.
5. What is the purpose of the ring oscillator test structure.
MUX LAYOUT AND GATE LEVEL SCHEMATIC

25 Transistors

\[ I_0, I_1, I_2, I_3 \]

\[ Q = A'B'I_0 + A'B'I_1 + AB'I_2 + ABI_3 \]
PMOS 4-INPUT MULTIPLEXER
In PMOS logic low is 0 volts, logic high is -Vcc

PMOS, Vcc = -10 Volts
In PMOS logic low is 0 volts, logic high is $-V_{cc}$.
PMOS ANALOG MUX