SPICE Model Parameters for RIT MOSFET’s

Dr. Lynn Fuller
Microelectronic Engineering
Rochester Institute of Technology
82 Lomb Memorial Drive
Rochester, NY 14623-5604
Tel (585) 475-2035
Fax (585) 475-5041

Dr. Fuller’s Webpage: http://people.rit.edu/lffeee
Email: Lynn.Fuller@rit.edu
Dept Webpage: http://www.microe.rit.edu
OUTLINE

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Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, Level 7, Level 48, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.
If we understand the Level 1 model we can better understand the other models. The Level 1 model by Schichman and Hodges uses basic device physics equations for MOSFET threshold voltage and drain current in the saturation and non-saturation regions of operation. Mobility is assumed to be a function of total doping concentration only and a parameter called LAMBDA is used to model channel length modulation.
where ID is a dependent current source using the equations on the next page
RIT MOSFET SPICE Parameters

SPICE LEVEL-1 EQUATIONS FOR UO, VT AND ID

Mobility:

\[ \mu = \mu_{\text{min}} + \frac{(\mu_{\text{max}} - \mu_{\text{min}})}{\left\{1 + (N/N_{\text{ref}})\alpha\right\}} \]

Threshold Voltage:

\[ V_{\text{TO}} = \Phi_{\text{ms}} - q \frac{\text{NSS/Cox}’}{\pm 2[\Phi F]} + \pm 2 (q\varepsilon_s \text{NSUB} [\Phi F])^{0.5}/Cox’ \]

Drain Current:

Non-Saturation

\[ I_D = \mu W \frac{\text{Cox’}}{L} (V_g - V_t - \frac{V_d}{2}) V_d (1 + \lambda V_d) \]

Saturation

\[ I_{\text{Dsat}} = \mu W \frac{\text{Cox’}}{2L} (V_g - V_t)^2 (1 + \lambda V_d) \]

Where:

- \( \mu \): Mobility
- \( \mu_{\text{min}} \): Minimum Mobility
- \( \mu_{\text{max}} \): Maximum Mobility
- \( N_{\text{ref}} \): Reference Doping
- \( \alpha \): Doping Sensitivity Parameter
- \( V_{\text{TO}} \): Threshold Voltage
- \( W \): Channel Width
- \( L \): Channel Length
- \( \Phi_{\text{ms}} \): Source-Scratch Potential
- \( \Phi_{F} \): Fermi Potential
- \( \lambda \): Substrate Conductivity
- \( \varepsilon_s \): Relative Permittivity
- \( \varepsilon_0 \): Vacuum Permittivity
- \( q \): Electron Charge
- \( k_B \): Boltzmann Constant
- \( T \): Temperature
- \( N_{\text{SUB}} \): Substrate Impurity Density
- \( n_i \): Substrate Carrier Density
- \( kT/q \): Thermal Voltage
- \( N_{\text{DD}} \): Doping Density
- \( N_{\text{LD}} \): Doping Level
- \( Cox’ \): Capacitance
- \( n_{\text{SH}} \): Surface Hole Density
- \( n_{\text{EX}} \): Extrinsic Carrier Density

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Body Effect coefficient GAMMA or $\gamma$:

$$
\gamma = \frac{1}{C_{ox}'} \sqrt{2q\varepsilon_{Si}N_A}
$$

$$
V_{T_{lc}} = \Phi_{MS} - \frac{Q_{SS}}{C_{ox}'} + 2\phi_F + \gamma \sqrt{2\phi_F} + V_{SB}
$$
**RIT MOSFET SPICE Parameters**

**CHANNEL LENGTH MODULATION**

Channel Length Modulation Parameter $\lambda$

$\lambda = \text{Slope/ } I_{dsat}$

$I_{dsat} = \mu W C_ox' (V_g-V_t)^2 (1+ \lambda V_{ds})$ 

$\frac{1}{2L}$

NMOS Transistor in Saturation Region

DC Model, $\lambda$ is the channel length modulation parameter and is different for each channel length, $L$. Typical value might be 0.02.

$\lambda = \text{LAMBDA in SPICE models}$
### RIT MOSFET SPICE Parameters

#### Lambda Versus Channel Length

<table>
<thead>
<tr>
<th>µA UNIT</th>
<th>SLOPE</th>
<th>IDSAT</th>
<th>W</th>
<th>L</th>
<th>PMOS</th>
<th>NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>205</td>
<td>4.9</td>
<td>6.8</td>
<td>32</td>
<td>2</td>
<td>0.144118</td>
<td>0.132308</td>
</tr>
<tr>
<td>71</td>
<td>2</td>
<td>7.1</td>
<td>32</td>
<td>4</td>
<td>0.056338</td>
<td>0.026761</td>
</tr>
<tr>
<td>56</td>
<td>1.8</td>
<td>7.3</td>
<td>32</td>
<td>6</td>
<td>0.049315</td>
<td>0.011429</td>
</tr>
<tr>
<td>34</td>
<td>1.2</td>
<td>7.5</td>
<td>32</td>
<td>8</td>
<td>0.032</td>
<td>0.013889</td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>7</td>
<td>32</td>
<td>16</td>
<td>0.028571</td>
<td>0.005556</td>
</tr>
<tr>
<td>8.8</td>
<td>0.8</td>
<td>7.6</td>
<td>32</td>
<td>32</td>
<td>0.021053</td>
<td>0.004196</td>
</tr>
<tr>
<td>415</td>
<td>4.3</td>
<td>6.5</td>
<td>32</td>
<td>2</td>
<td>0.132308</td>
<td>0.013889</td>
</tr>
<tr>
<td>137</td>
<td>0.95</td>
<td>7.1</td>
<td>32</td>
<td>4</td>
<td>0.026761</td>
<td>0.013889</td>
</tr>
<tr>
<td>91</td>
<td>0.4</td>
<td>7</td>
<td>32</td>
<td>6</td>
<td>0.011429</td>
<td>0.004196</td>
</tr>
<tr>
<td>137</td>
<td>0.5</td>
<td>7.2</td>
<td>32</td>
<td>8</td>
<td>0.013889</td>
<td>0.004196</td>
</tr>
<tr>
<td>27</td>
<td>0.2</td>
<td>7.2</td>
<td>32</td>
<td>16</td>
<td>0.005556</td>
<td>0.004196</td>
</tr>
<tr>
<td>15</td>
<td>0.15</td>
<td>7.15</td>
<td>32</td>
<td>32</td>
<td>0.004196</td>
<td>0.004196</td>
</tr>
</tbody>
</table>

Need different model for each different length transistor

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**SPICE LEVEL-1 PARAMETERS**

SPICE LEVEL 1 MODEL FOR MOS TRANSISTORS:

1. LEVEL=1
2. VTO
3. KP
4. GAMMA
5. PHI
6. LAMBDA
7. RD
8. RS
9. CBD
10. CBS
11. IS
12. PB
13. CGSO
14. CGDO
15. CGBO
16. RSH
17. CJ
18. MJ
19. CJSW
20. MJSW
21. JS
22. TOX
23. NSUB
24. NSS
25. NFS
26. TPG
27. XJ
28. LD
29. UO
30. LAMBDA
31. PB
32. MJ
33. NSS
34. NSUB
35. UO

36. 37. 38. 39. 40. 41. PARAMETERS FOR SHORT CHANNEL AND NOISE (Use Defaults)
1. LEVEL=1 Schichman-Hodges Model

2. VTO zero bias threshold voltage (Do not use, let SPICE calculate from Nsub, TOX unless an VT adjust ion implant is used to set VTO at some value)

3. KP transconductance parameter (Do not use, let SPICE calculate from UO, COX')

\[ KP = UO \cdot COX' = UO \cdot \epsilon_r \epsilon_0 / TOX \]
4. GAMMA bulk threshold parameter (Do not use, let SPICE calculate from UO,COX’)

\[ \text{GAMMA} = [2q \varepsilon_{\text{si}} \varepsilon_0 \text{NSUB}/C’_\text{ox}^2]^{1/2} \]

where \( \varepsilon_{\text{si}} \varepsilon_0 = (11.7)(8.85 \times 10^{-12}) \) and \( q = 1.6 \times 10^{-19} \)

5. PHI is the semiconductor potential, Intrinsic Level to Fermi Level difference in Volts (Do not use, let SPICE calculate from NSUB)

\[ \text{PHI} = 2[\Phi_F] = 2 \left( \frac{KT}{q} \right) \ln \left( \frac{\text{NSUB}}{n_i} \right) \]

where \( KT/q = 0.026 \)

\( n_i = 1.45 \times 10^{10} \)

6. LAMBDA is the channel length modulation parameter, Slope in saturation region divided by Idsat

\[ \lambda = \frac{\text{Slope}}{\text{Idsat}} \]

\[ \text{Slope} \rightarrow \text{Saturation Region} \]

\[ \text{Idsat} \]

\[ \text{Vd1} \quad \text{Vd2} \quad +V_{\text{gs}} \quad +V_{\text{ds}} \]

\[ +2 \quad +3 \quad +4 \quad +5 \]
7. RD the series drain resistance can either be given as a resistance value or through RSH the drain/source sheet resistance and the number of squares NRS. NRS: Is from the device layout. RSH: Is measured by four point probe or Van Der Pauw structures
(Do not use, let SPICE calculate from sheet resistance, RSH, and number of squares in drain, NRD)

8. RS is the series source resistance can either be given as a resistance value or through RSH the drain/source sheet resistance and the number of squares NRS. NRS: Is from the device layout. RSH: Is measured by four point probe or Van Der Pauw structures
(Do not use, let SPICE calculate from sheet resistance, RSH, and number of squares in source, NRS)
9. CBD zero bias bulk to drain junction capacitance (Do not use, let SPICE calculate from CJ and CJSW and AD (Area of Drain) and PD (Perimeter of Drain))
   \[ CBD = CJ \cdot AD + CJSW \cdot PD \]

10. CBS zero bias bulk to source junction capacitance (Do not use, let SPICE calculate from CJ and CJSW and AS (Area of Source) and PD (Perimeter of Source))
    \[ CBS = CJ \cdot AS + CJSW \cdot PS \]

11. IS is the bulk junction saturation current in the ideal diode equation.
    \[ I = IS \cdot \exp \left( \frac{qV_A}{kT} \right) - 1 \]
    (Do not use, let SPICE calculate from JS and AD (Area of Drain) and AS (Area of Source))
    \[ IS = JS \cdot (AD + AS) \]

12. PB is the junction built in voltage
    \[ PB = \frac{(KT)}{q} \ln \left( \frac{NSUB}{ni} \right) + 0.56 \]
13. CGSO is the gate-to-source overlap capacitance (per meter channel width)
   \[ CGSO = Cox' \text{ (mask overlap in L direction + LD)} \ F/m \]

14. CGDO is the gate-to-drain overlap capacitance (per meter channel width)
   \[ CGDO = Cox' \text{ (mask overlap in L direction + LD)} \ F/m \]

15. CGBO is the gate-to-bulk overlap capacitance (per meter channel length)
   \[ CGBO = C_{\text{field_oxide}} \star \text{mask overlap in W direction} \ F/m \]

\[ C_{\text{field_oxide}} = \varepsilon_r \varepsilon_o / X_{\text{FieldOX}} \]
16. RSH is the drain and source diffusion sheet resistance. Measured from four point probe or Van Der Pauw structures.

17. CJ is the zero bias bulk junction bottom capacitance per square meter of junction area. \( CJ = \frac{\varepsilon_r \varepsilon_0}{W} \) where \( W \) is width of space charge layer.

\[
CJ = \frac{\varepsilon_r \varepsilon_0}{W} \left(2\varepsilon_r \varepsilon_0 \frac{(\Psi_o - VA)}{qN_{sub}}\right)^m \text{ F/m}^2
\]

where \( \Psi_o = PB = \frac{(KT/q)}{\ln (N_{SUB}/n_i)} + 0.56 \)

\( m = \) junction grading coefficient = 0.5

18. MJ is the junction grading coefficient = 0.5

19. CJSW is the zero bias bulk junction sidewall capacitance per meter of junction perimeter. \( CJSW = CJ XJ \)

20. MJSW is the junction grading coefficient = 0.5

21. JS is the bulk junction saturation current density in Amperes per square meter

\[
JS = q n_i^2 \frac{(D_p/N_d L_p + D_n/ N_a L_n)}{\text{ where } D = (KT/q) \mu \text{ and } L = (D\tau)^{0.5}}
\]
22. TOX is the gate oxide thickness, measured by ellipsometer or reflectance spectroscopy (Nanospec).

23. NSUB the substrate doping is given by the wafer manufacturer or measured by four point probe technique. In both cases NSUB is given indirectly by the resistivity, Rho. Rho = 1/(qµ(N)N) where q = 1.6E-19 coul, N is the substrate doping NSUB, µ(N) is the mobility, a function of N.

**Empirical Equation:**

\[ \mu = \mu_{\text{min}} + (\mu_{\text{max}} - \mu_{\text{min}}) \left\{ 1 + \left( \frac{N}{N_{\text{ref}}} \right)^\alpha \right\} \]

<table>
<thead>
<tr>
<th>Electron</th>
<th>Hole</th>
</tr>
</thead>
<tbody>
<tr>
<td>µmin</td>
<td>92</td>
</tr>
<tr>
<td>µmax</td>
<td>1360</td>
</tr>
<tr>
<td>Nref</td>
<td>1.3E17</td>
</tr>
<tr>
<td>α</td>
<td>0.91</td>
</tr>
</tbody>
</table>
24. NSS: The surface state density is a parameter used in the calculation of the zero-bias threshold voltage (ie. Vsource = Vsubstrate), VT0 is obtained from transistor curves.

\[
VTO = \Phi_{ms} - q \frac{NSS}{Cox'} - 2 \Phi_F - 2 \left( q\varepsilon_s NSUB \Phi_F \right)^{0.5}/Cox'
\]

\[
\Phi_F = \left( \frac{KT}{q} \right) \ln \left( \frac{NSUB}{ni} \right) \quad \text{where} \quad ni = 1.45\text{E10} \quad \text{and} \quad KT/q = 0.026
\]

\[
\Phi_{ms} = \Phi_m - (X + Eg/2 - \Phi_F) \quad \text{where} \quad \Phi_m = \text{gate work function}
\]

\[
X = 4.15 \text{ eV}, \quad Eg = 1.12 \text{ eV}
\]

\[
\varepsilon_s = \varepsilon_r \varepsilon_o = 11.7 \varepsilon_o
\]

Since everything is known

\[
Cox' = \varepsilon_r \varepsilon_o / TOX = 3.9 \varepsilon_o / TOX
\]

in equations above, NSS can be calculated

25. NFS is the fast surface state density, usually left at zero.
26. TPG is the type of gate. for aluminum TPG=0, for n+ poly TPG = 1, for p+ poly TPG= -1
27. XJ metallurgical junction depth, measured by groove and stain techniques.
28. LD lateral diffusion distance, inferred from process knowledge
29. UO is the surface mobility taken as 1/2 the bulk mobility or extracted to give correct Id value on measured Id vs Vds characteristics in the saturation region. For best results make measurements on a transistor with large channel length so that $\lambda$ is small and the lateral diffusion can be neglected.

$$I_{D_{\text{sat}}} = \mu W Cox' (Vg-Vt)^2 (1+ \lambda Vds)$$

$$2L$$

30. - 41. Parameters associated with short channel devices and noise in MOSFETs
2\(^{\text{nd}}\) generation MOSFET models improve over the Level 1 models because they model sub-threshold current, mobility as a function of vertical and lateral electric field strength, threshold voltage reduction as a function of drain voltage or drain induced barrier lowering (DIBL). This model has separate equations for drain current for different regions of operation. The discontinuity at the transition points can make problems in program convergence during circuit simulation.
TERADA-MUTA METHOD FOR EXTRACTING $L_{eff}$ and $R_d$ 

Terada-Muta Method for $L_{eff}$ and $R_d$

In the linear region ($V_D$ is small):

$$I_D = \frac{\mu W C_{ox}'}{(V_g - V_t - V_D/2) \cdot V_D}$$

$$L_{eff} = L_m - \Delta L$$

where $\Delta L$ is correction due to processing

$L_m$ is the mask length

$$R_m = \frac{V_D}{I_D} = \text{measured resistance}$$

$$= \frac{L_m}{(\mu W C_{ox'} (V_g - V_t)) - \Delta L/ \mu W C_{ox'} (V_g - V_t)}$$

so measure $R_m$ for different channel length transistors and plot $R_m$ vs $L_m$

where $R_m = \text{intersect find value for } \Delta L \text{ and } R_d$

Then $L_{eff}$ can be calculated for each different length transistor

from $L_{eff} = L_m - \Delta L$
The mobility used in the equations for \( I_{ds} \) is the effective mobility, \( U_{eff} \). Starting with \( U_0 \) from level 1, \( U_{eff} \) is found. The parameter \( \Theta \) is introduced to model mobility degradation due to high vertical electric fields (larger values of \( V_{gs} - V_{TO} \)).

\[
U_{eff}^* = \frac{U_0}{1 + \Theta (V_{gs} - V_{TO})}
\]

Measure \( I_{ds} \) for a wide transistor with low value of \( V_{ds} \) and large value of \( V_{gs} \) and using \( L_{eff} \) from Terata-Muta method and \( \lambda \) from level 1, calculate \( \Theta \) from these two equations.

\[
I_{dsat} = \frac{U_{eff} W \ Cox'}{(V_{g} - V_{t})^{2} (1 + \lambda V_{ds})}{2L_{eff}}
\]

Warning: Curvature also due to \( R_{DS} \) so \( V_{ds} \) is \((V_{applied} - R_{ds}*I_{dsat})\) requires an iterative approach to find \( \Theta \).
The parameter $V_{MAX}$ is introduced to model the decrease in mobility at higher $V_{ds}$ due to velocity saturation. Ideally, carrier velocity is directly proportional to the applied electric field. However, at very high lateral electric fields, $E_x$, this relationship ceases to be accurate - the carrier velocity saturates at $V_{MAX}$.

\[ \nu = UO \frac{V_{ds}}{E_x} \]

Where, $V_{de} = \min(V_{ds}, V_{dsat})$

\[ U_{eff} = \frac{UO}{(1 + \Theta (V_{gs} - V_{TO})) \left( 1 + UO \frac{V_{de}}{V_{MAX} L_{eff}} \right)} \]

Where, $V_{de}$ = \min (V_{ds}, V_{dsat})

Note: other models (equations) for mobility exist and use parameters such as UCRIT, UEXP, ULTRA, ECRIT, ESAT
The parameter ETA is used to describe DIBL (Drain Induced Barrier Lowering) resulting in a modification to the LEVEL 1 equation for threshold voltage.

\[
V_{TO} = \Phi_{ms} - \phi_{\eta} - q \frac{N_{SS}}{C_{ox'}} - 2 \Phi - 2 (q\epsilon_s N_{SUB} \Phi)^{0.5}/C_{ox'}
\]

\[
\phi_{\eta} = \frac{(- 8.14E-22) \cdot \eta}{C_{ox'} L_{eff}^3} \quad V_{ds}
\]
DELTA is introduced to model narrow channel effects on threshold voltage. The parameter WD (channel width reduction from drawn value) is used to calculate the effective channel width. DELTA is used in the calculation of threshold voltage.

\[
\text{DELTA} = \frac{q \text{NSUB} Xds^2}{\varepsilon_0 \varepsilon_i 2 \text{PHI}}
\]

Note: a dimensionless number typically \(~3\)
KAPPA is channel length modulation parameter.

KAPPA is calculated = \[
\left(\frac{qN_{\text{sub}}}{2\varepsilon_{\text{o}}\varepsilon_{\text{r}}}\right)\left(1-\frac{I_{\text{dsat}}}{I'}\left(L-2L_{D}-X_{dso}-X_{ds}\right)\right)^2/(V_{d2}-V_{\text{dsat}})^{0.5}
\]

Measure $I'$ at large $V_d$, and $I_{\text{dsat}}$ at $V_{\text{dsat}}$, Kappa has units of $1/V$ typical value ~0.1
SPICE LEVEL 3 MODEL PARAMETERS FOR MOS TRANSISTORS:

- **Control Level**: 3
- **Process TPG**: 1
  - 1 if gate is doped opposite of channel, -1 if not
- **Process TOX**: Gate Oxide Thickness
- **Process NSUB**: Channel doping concentration
- **Process XJ**: Drain/Source Junction Depth
- **Process PB**: PB is the junction built in voltage
- **W and L WD**: Decrease in Width from Drawn Value
- **DC UO**: Zero Bias Low Field Mobility
- **DC VTO**: Measured threshold voltage, long wide devices
- **DC THETA**: Gate Field Induced Mobility Reduction
- **DC DELTA**: Narrow Channel Effect on the Threshold Voltage
- **DC VMAX**: Maximum Carrier Velocity
- **DC ETA**: DIBL Coefficient
- **DC KAPPA**: Channel Length Modulation Effect on Ids
- **DC NFS**: Surface State Density
PARAMETERS FOR SPICE LEVEL 3

Diode & Resistor RS       Source Series Resistance
Diode & Resistor RD       Drain Series Resistance
AC   CGDO                 Zero Bias Gate-Source Capacitance
AC   CGSO                 Zero Bias Gate-Drain Capacitance
AC   CGBO                 Zero Bias Gate-Substrate Capacitance
AC   CJ                    
Temp                      - more
Noise                     - more
Tunneling                  
- more
Berkeley SPICE third generation SPICE models are called BSIM3. These models for transistors use equations that are continuous over the entire range of operation (sub-threshold, linear region and saturation region). The equations for mobility are improved. Equations for temperature variation, stress effects, noise, tunneling have been added and/or improved. BSIM3 is presently the industry standard among all these models. It represents a MOSFET with many electrical and structural parameters, among which, only \( W \) and \( L \) are under the control of a circuit designer. All the rest are fixed for all MOSFETs integrated in a given fabrication technology, and are provided to the designer as an “untouchable” deck of device parameters. (There are over 200 parameters in some versions of BISM3 models)
\[ V_{th} = VTH0 + K1 \cdot \left( \sqrt{\phi_s - V_{bseff} - \phi_s} \right) - K2 \cdot V_{bseff} \]
\[ - K1 \cdot \left( \sqrt{1 + \frac{\text{NLX}}{L_{eff}}} - 1 \right) \cdot \sqrt{\phi_s} + (K3 + K3b \cdot V_{bseff}) \cdot \frac{\text{TOX}}{W_{eff} + W_0} \cdot \phi_s \]
\[ - DVT0 \cdot \left( \exp \left( -DVT1 \cdot \frac{L_{eff}}{2l_t} \right) + 2 \cdot \exp \left( -DVT1 \cdot \frac{L_{eff}}{l_t} \right) \right) \cdot \left( V_{bi} - \phi_s \right) \]
\[ - \left( \exp \left( -\text{DSUB} \cdot \frac{L_{eff}}{2l_{t0}} \right) + 2 \cdot \exp \left( -\text{DSUB} \cdot \frac{L_{eff}}{l_{t0}} \right) \right) \cdot (\text{ETA0} + \text{ETAB} \cdot V_{bseff}) \cdot V_{ds} \]
\[ - DVT0W \cdot \left( \exp \left( -DVT1W \cdot \frac{L_{eff} \cdot W_{eff}}{2l_{tw}} \right) + 2 \cdot \exp \left( -DVT1W \cdot \frac{L_{eff} \cdot W_{eff}}{l_{tw}} \right) \right) \cdot (V_{bi} - \phi_s) \]
MOBMOD = 1

\[
\mu_{\text{eff}} = \frac{U_0}{1 + (U_A + U_C \cdot V_{b\text{seff}}) \cdot \left( \frac{V_{g\text{st}0ff} + 2 \cdot V_{\text{th}}}{\text{TOX}} \right) + U_B \cdot \left( \frac{V_{g\text{st}0ff} + 2 \cdot V_{\text{th}}}{\text{TOX}} \right)^2}
\]

UA, UB and UC are empirically fit and replace THETA and VMAX used in LEVEL 3

Effective Vgs - Vth

\[
V_{g\text{st}0ff} = \frac{2 \cdot n \cdot V_t \cdot \ln \left( 1 + \exp \left( \frac{V_g - V_{\text{th}}}{2 \cdot n \cdot V_t} \right) \right)}{1 + 2 \cdot n \cdot \text{COX} \cdot \left( \frac{2 \cdot \phi_s}{q \cdot \varepsilon_{\text{si}} \cdot \text{NCH}} \cdot \exp \left( \frac{V_g - V_{\text{th}} - 2 \cdot V_{\text{OFF}}}{2 \cdot n \cdot V_t} \right) \right)}
\]

n = 1 + NFACTOR *Cd/COX + ((CDSC + CDSCD*Vds + CDSCB*Vbseff) – (exp(-DVT1*Leff/2lt) + 2exp(-DVT1*Leff/lt)))/COX + CIT/COX
Effective $V_{ds}$

$$V_{dseff} = V_{dsat} - \frac{1}{2} \cdot (V_{dsat} - V_d - \text{DELTA} - \sqrt{(V_{dsat} - V_d - \text{DELTA})^2 + 4 \cdot \text{DELTA} \cdot V_{dsat}})$$

Drain Current

$$I_{ds} = \frac{I_{dso}}{R_{ds} \cdot I_{dso}} \cdot \left(1 - \frac{V_d - V_{dseff}}{V_A} \right) \cdot \left(1 - \frac{V_d - V_{dseff}}{V_{ASCBE}} \right)$$

$$I_{dso} = \frac{W_{eff} \cdot \mu_{eff} \cdot \text{COX} \cdot V_{gseff} \cdot \left(1 - A_{bulk} \cdot \frac{V_{dseff}}{2 \cdot (V_{gseff}^2 - V_t^2)} \right) \cdot V_{dseff}}{L_{eff} \cdot [1 + V_{dseff} / (E_{sat} \cdot L_{eff})]}$$

$$V_A = V_{Asat} = \left(1 + \frac{PVAG \cdot V_{gseff}}{E_{sat} \cdot L_{eff}} \right) \cdot \left(\frac{1}{V_{ACL}^{\text{ACL}}} - \frac{1}{V_{ADIBL}^{\text{ADIBL}}} \right)^{-1}$$

$$V_{ACL} = \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} \cdot V_{gseff}}{PCLM \cdot A_{bulk} \cdot E_{sat} \cdot L_{eff} \cdot (V_d - V_{dseff})}$$
SPICE LEVEL-49 EQUATIONS FOR ID (cont)

\[ V_{ADIBLC} = \frac{(V_{gsteff} + 2 \cdot V_t)}{\theta_{rout} \cdot (1 + PDIBLBC \cdot V_{beff}) \cdot \left(1 - \frac{A_{bulk} \cdot V_{dsat}}{A_{bulk} \cdot V_{dsat} + V_{gsteff} + 2 \cdot V_t}\right)} \]

\[ \theta_{rout} = PDIBLC1 \cdot \left[ \exp\left(-DROUT \cdot \frac{L_{off}}{2 \cdot l_{to}}\right) + 2 \cdot \exp\left(-DROUT \cdot \frac{L_{off}}{l_{to}}\right) \right] + PDIBLC2 \]

\[ \frac{1}{V_{A3CBE}} = \frac{PSCBE2}{L_{eff}} \cdot \exp\left(\frac{-PSCBE1 \cdot l_{it}}{V_{ds} - V_{dsaff}}\right) \]

\[ V_{A_{sat}} = \frac{E_{sat} \cdot L_{off} + V_{dsat} + 2 \cdot R_{ds} \cdot VSAT \cdot COX \cdot W_{eff} \cdot V_{gsteff} \cdot \left[1 - \frac{A_{bulk} \cdot V_{dsat}}{2 \cdot (V_{gsteff} + 2 \cdot V_t)}\right]}{2/\lambda - 1 + R_{ds} \cdot VSAT \cdot COX \cdot W_{off} \cdot A_{bulk}} \]

\[ l_{it} = \sqrt{\frac{\varepsilon_{si} \cdot TOX \cdot XJ}{\varepsilon_{ox}}} \]
<table>
<thead>
<tr>
<th>Control</th>
<th>LEVEL=49</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>MOBMOD=1 Mobility model selector choice</td>
</tr>
<tr>
<td>Control</td>
<td>CAPMOD=1 Capacitor model selector choice</td>
</tr>
<tr>
<td>Process</td>
<td>TOX Gate Oxide Thickness</td>
</tr>
<tr>
<td>Process</td>
<td>XJ Drain/Source Junction Depth</td>
</tr>
<tr>
<td>Process</td>
<td>NCH Channel Surface doping concentration</td>
</tr>
<tr>
<td>Process</td>
<td>NSUB Channel doping concentration</td>
</tr>
<tr>
<td>Process</td>
<td>XT Distance into the well where NCH is valid</td>
</tr>
<tr>
<td>Process</td>
<td>NSF Fast Surface State Density</td>
</tr>
<tr>
<td>Process</td>
<td>NGATE Gate Doping Concentration</td>
</tr>
<tr>
<td>W and L</td>
<td>WINT Isolation Reduction of Channel Width</td>
</tr>
<tr>
<td>W and L</td>
<td>LINT Source/Drain Underdiffusion of Gate</td>
</tr>
</tbody>
</table>

Note: only some of the few hundred parameters
### RIT MOSFET SPICE Parameters

#### PARAMETERS FOR SPICE BSIM3 LEVEL 49

| DC/VTH0 | Threshold voltage, Long, Wide Device, Zero Substrate Bias = VTO in level 3 |
| DC/U0   | Low Field Mobility, UO in level 3 |
| DC/PCLM | Channel Length Modulation Parameter |
| Diode & Resistor RSH | Drain/Source sheet Resistance |
| Diode & Resistor JS | Bottom junction saturation current per unit area |
| Diode & Resistor JSW | Side wall junction saturation current per unit length |
| Diode & Resistor CJ | Bottom Junction Capacitance per unit area at zero bias |
| Diode & Resistor MJ | Bottom Junction Capacitance Grading Coefficient |
| Diode & Resistor PB | PB is the junction built in voltage |
| Diode & Resistor CJSW | Side Wall Junction Capacitance per meter of length |
| Diode & Resistor MJSW | Side Wall Junction Capacitance Grading Coefficient |
| AC/CGSO | Zero Bias Gate-Source Capacitance per meter of gate W |
| AC/CGDO | Zero Bias Gate-Drain Capacitance per meter of gate W |
| AC/CGBO | Zero Bias Gate-Substrate Capacitance per meter of gate L |

Note: only some of the few hundred parameters
## RIT MOSFET SPICE Parameters

### EXCEL SPREADSHEET SPICE PARAMETER CALCULATOR

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ROCHESTER INSTITUTE OF TECHNOLOGY</td>
<td>SPICE Parameter Calculator.xls</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>MICROELECTRONIC ENGINEERING</td>
<td>1/18/2007</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>CALCULATION OF MOSFET SPICE PARAMETERS</td>
<td>DR. LYNN FULLER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>To use this spreadsheet change the values in the white boxes. The rest of the sheet is protected and should not be changed unless you are sure of the consequences. The calculated results are shown in the purple boxes.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CONSTANTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>$T$ = 300 K</td>
<td>$E_{ox}$ D0</td>
<td>0.76 cm^2/Vs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>$K_T/q$ = 0.026 volts</td>
<td>$E_{ox}$ E3</td>
<td>3.46 eV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>$n_0 = 1.45 \times 10^{10}$ cm^{-3}</td>
<td>$E_{ph}$ D0</td>
<td>3.85 cm^2/Vs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>$E_0 = 8.85 \times 14$ V/cm</td>
<td>$E_{ph}$ E3</td>
<td>3.66 eV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>$F_a = 11.7$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>$E_{max} = 1.9$</td>
<td>Carrier Velocity Saturation covers 350 to 250 cm/s, extracted values can be artificially 2 times higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>$V_{sat} = 4.5$ volts</td>
<td>Critical value of electric field $E_{cr}$ of $1.5$ to $25$ V/cm for electrons, $350$ to $15$ V/cm for holes</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>$q = 1.6 \times 10^{-19}$ coul</td>
<td>$E_{g} = 1.124$ volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### INTRODUCTION

This spreadsheet calculates on a panel level page, these and BSIM3 SPICE parameters from details known about the process parameters, device layout and fabrication history. Level one spice parameters assume mobility is a function of total impurity concentration and temperature only. Level one uses the parameter $LAMBDA$ for channel length modulation. Different equations are used to calculate $I_D$ in the saturation and sub-threshold regions of operation.

The level three SPICE models is derived from the level one model with some additional parameters to better account for the decrease in carrier mobility for high vertical and lateral electric fields. The level three model also allows the user to account for narrow channel effects, drain induced barrier lowering (DBL), and gives better sub-threshold characteristics. For example the parameter $LAMBDA$ is replaced by a more complex model using the parameter $V_{MAX}$ and $K_{TPA}$. The low field mobility value $DOC$ is modified for high gate electric fields with parameter $THETA$, and modified for high lateral electric fields through the $V_{MAX}$ parameter. Different equations are used to calculate $I_D$ in the saturation, non-saturation and sub-threshold regions of operation.

The BSIM3 SPICE parameters are derived from the level one and three parameters. BSIM models have hundreds of parameters used to fully describe DC and AC device operation, temperature effects, noise, stress effects and more. Most of the parameters can only be determined from measured device performance. In this spreadsheet the BSIM parameters are derived from level one and level three parameters. All other parameters are not specified and the default values are used. The single equation for $I_D$ is used that is valid in saturation, non-saturation and sub-threshold regions of operation, making convergence during circuit simulation more reliable.

### REFERENCES
- CMOS: Introduction to VLSI Technology, Ch. 5 From Silvaco International

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### Layout Parameters

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
</tr>
</thead>
</table>
| 44 | LAYOUT PARAMETERS | 45 | (assure source and drain are symmetrical) | 46 | W | 16 | um | 47 | V | 10 | cm
| 48 | Area of Drain Source | 96 | cm² | 49 | Perimeter of Drain Source | 44 | cm | 50 | # squares between Contact and Channel | 0.1 ± 0.1 | cm² | 51 | # squares between LDD/ + and Channel | 0.025 |

### Process Parameters

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>52</td>
<td>Aluminium gate</td>
<td>0</td>
<td>53</td>
<td>n+ Poly gate</td>
<td>1</td>
<td>select one</td>
<td>54</td>
<td>p+ Poly gate</td>
<td>0</td>
<td>select one</td>
<td>55</td>
</tr>
<tr>
<td>57</td>
<td>V select Dose (+ for Donor, – for Phosphorus)</td>
<td>0.002±0.1</td>
<td>cm²</td>
<td>58</td>
<td>Gate Oxide Thickness</td>
<td>150</td>
<td>Å</td>
<td>59</td>
<td>NBS</td>
<td>3.0±0.1</td>
<td>cm²</td>
</tr>
<tr>
<td>61</td>
<td>Well Dose</td>
<td>2.0±0.3</td>
<td>cm²</td>
<td>62</td>
<td>Well Drive Time</td>
<td>710</td>
<td>min</td>
<td>63</td>
<td>Well Drive Temperature</td>
<td>110</td>
<td>°C</td>
</tr>
<tr>
<td>64</td>
<td>LDD D/S Dose</td>
<td>2.5±0.3</td>
<td>cm²</td>
<td>65</td>
<td>LDD D/S Drive Time</td>
<td>50</td>
<td>min</td>
<td>66</td>
<td>LDD D/S Drive Temperature</td>
<td>1000</td>
<td>°C</td>
</tr>
<tr>
<td>67</td>
<td>Field Oxide Thickness</td>
<td>6000</td>
<td>Å</td>
<td>68</td>
<td>Minority Carrier Lifetime in the well</td>
<td>1</td>
<td>μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>69</td>
<td>D/S Dose (N+ or P+)</td>
<td>2.0±0.3</td>
<td>cm²</td>
<td>70</td>
<td>D/S Width of Space Charge Layer at Zero Bias, X0</td>
<td>0.152</td>
<td>cm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>71</td>
<td>Off =</td>
<td>2.0±0.3</td>
<td>cm²</td>
<td>72</td>
<td>Built-In Voltage for D/S junction</td>
<td>0.05</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>73</td>
<td>Junction, reverse bias current density, JS</td>
<td>3.2±0.2</td>
<td>A/cm²</td>
<td>74</td>
<td>Junction capacitance for D/S at zero bias</td>
<td>6.0±0.8</td>
<td>F/cm²</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>Lambda, Calculated, (cm²/Quanta)</td>
<td>0.05</td>
<td>cm²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Measured Transistor Values

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>76</td>
<td>Vdd</td>
<td>5</td>
<td>volts</td>
<td>77</td>
<td>Calculated Spce Parameters from Measured Values</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>78</td>
<td>Magnitude of IDS at Vgs = 0</td>
<td>4.41</td>
<td>mAmps</td>
<td>79</td>
<td>Lambda</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>Magnitude of IDS at Vgs = 0, Vds = Vdd</td>
<td>5.12</td>
<td>mAmps</td>
<td>0.03</td>
<td>Iprods</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>81</td>
<td>VTO (+ for n channel, – for p channel)</td>
<td>1.1</td>
<td>volts</td>
<td>82</td>
<td>VTO measured</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>83</td>
<td>D/S Sheet Resistance</td>
<td>39.2</td>
<td>Ω/μm²</td>
<td>84</td>
<td>JS, Isub-min/min Area of a beam measured</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>Lambda</td>
<td>0.03</td>
<td>1/Ωvamps</td>
<td>86</td>
<td>Rθ measured</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Inputs and Results**

---

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# RIT MOSFET SPICE Parameters

## PARAMETERS FOR SPICE LEVEL 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>SPICE Parameter</th>
<th>Note: most parameters use D or 0 at end of parameter name (&quot;0th&quot; or &quot;Dth&quot;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Level</td>
<td>Using Process Parameter</td>
<td>Selects a model from a set of predefined models</td>
</tr>
<tr>
<td>2</td>
<td>YTO</td>
<td>1.93 volts</td>
<td>Zero Bias Threshold Voltage, enter value if threshold adjust implant is used</td>
</tr>
<tr>
<td>3</td>
<td>KP</td>
<td>2.30E-06 F/s/volt</td>
<td>Transconductance Parameter, KP = U0 * Em / C0x</td>
</tr>
<tr>
<td>4</td>
<td>GAMMA</td>
<td>0.12E+01</td>
<td>Bulk Threshold Parameter, GAMMA</td>
</tr>
<tr>
<td>5</td>
<td>FHI</td>
<td>0.412 volts</td>
<td>FHI is the Fermi potential, Intermate Level to Fermi Level difference</td>
</tr>
<tr>
<td>6</td>
<td>LAMBDA</td>
<td>0.381 L/mol</td>
<td>Channel length modulation parameter</td>
</tr>
<tr>
<td>7</td>
<td>RD</td>
<td>22.61 ohms</td>
<td>Channel Drain Resistance</td>
</tr>
<tr>
<td>8</td>
<td>RS</td>
<td>27.69 ohms</td>
<td>Source-Drain Resistance</td>
</tr>
<tr>
<td>9</td>
<td>CBD</td>
<td>3.02E+14 F</td>
<td>CBD zeroes built-in drain junction capacitance, CBD = CIAD + CIWF + FB</td>
</tr>
<tr>
<td>10</td>
<td>CES</td>
<td>3.02E+14 F</td>
<td>CES zeroes built-in source junction capacitance, CES = CIAD + CIWF + FB</td>
</tr>
<tr>
<td>11</td>
<td>IS</td>
<td>3.10E-18 A</td>
<td>D/S junction leakage current</td>
</tr>
<tr>
<td>12</td>
<td>PB</td>
<td>0.95 volts</td>
<td>PB is the junction built-in voltage, PB = (1/2) * (Vb / (NRSUB + 1))</td>
</tr>
<tr>
<td>13</td>
<td>CUD</td>
<td>2.46E-10 F/m</td>
<td>G = D overlap C (per channel width) CUD = Connect mask overlap in L direction + LD</td>
</tr>
<tr>
<td>14</td>
<td>COO</td>
<td>2.46E-10 F/m</td>
<td>G = D overlap C (per channel width) COO = Connect mask overlap in L direction + LD</td>
</tr>
<tr>
<td>15</td>
<td>CBO</td>
<td>7.55E-10 F/m</td>
<td>G = D overlap C (per channel length) CBO = Connect mask overlap in W direction + LD</td>
</tr>
<tr>
<td>16</td>
<td>PSH</td>
<td>1082.55 ohms</td>
<td>Sheet resistance of SD</td>
</tr>
<tr>
<td>17</td>
<td>CJ</td>
<td>6.00E+05 F/m^2</td>
<td>D/S Bottom junction capacitance/m^2</td>
</tr>
<tr>
<td>18</td>
<td>MN</td>
<td>0.5</td>
<td>Junction Grading Coefficient for base of D/S Junction</td>
</tr>
<tr>
<td>19</td>
<td>CBSW</td>
<td>1.26E+10 F/m</td>
<td>D/S side wall junction capacitance per meter of D/S perimeter</td>
</tr>
<tr>
<td>20</td>
<td>MSW</td>
<td>0.5</td>
<td>Junction Grading Coefficient for side of D/S Junction</td>
</tr>
<tr>
<td>21</td>
<td>RS</td>
<td>2.33E-08 ohms/m</td>
<td>D/S junction leakage current</td>
</tr>
<tr>
<td>22</td>
<td>TOX</td>
<td>3.10E-08 cm</td>
<td>Gate Oxide Thickness</td>
</tr>
<tr>
<td>23</td>
<td>NSSUB</td>
<td>1.45E+17 cm^-3</td>
<td>Bulk Doping</td>
</tr>
<tr>
<td>24</td>
<td>NSS</td>
<td>3.00E+11 cm^-2</td>
<td>Surface State Density as known from process knowledge</td>
</tr>
<tr>
<td>25</td>
<td>NFS</td>
<td>0</td>
<td>Fast Surface States, always set to zero</td>
</tr>
<tr>
<td>26</td>
<td>TPG</td>
<td>1</td>
<td>TPG is a gate doping offset of channel, -1 if gate doped same as channel, 0 if gate is aluminum</td>
</tr>
<tr>
<td>27</td>
<td>XC</td>
<td>0.43 cm</td>
<td>D/S Junction Depth</td>
</tr>
<tr>
<td>28</td>
<td>LD</td>
<td>0.05 cm</td>
<td>Linear Diffusion of D/S into the channel initially set to 50% of X0</td>
</tr>
<tr>
<td>29</td>
<td>H0</td>
<td>363 m</td>
<td>Will affect minority carrier mobility as well as surface concentration divided by two</td>
</tr>
</tbody>
</table>

---

**Model RITSUB1:**

**NMQS LEVEL 1**

- **HYTO:** 1.0
- **LAMBDA:** 0.031
- **PB:** 0.95
- **CUD:** 3.4E-10
- **COO:** 3.4E-10
- **CBO:** 7.55E-10
- **TOX:** 1.45E+17
- **NSSUB:** 1.54E+17
- **NSS:** 3E11

---

**Model RITSUB1:**

**PMS LEVEL 1**

- **HYTO:** 1.0
- **LAMBDA:** 0.031
- **PB:** 0.95
- **CUD:** 3.4E-10
- **COO:** 3.4E-10
- **CBO:** 7.55E-10
- **TOX:** 1.45E+17
- **NSSUB:** 1.54E+17
- **NSS:** 3E11

---

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### PARAMETERS FOR SPICE LEVEL 3

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Level</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>TF3</td>
<td>1</td>
<td>m</td>
</tr>
<tr>
<td>3</td>
<td>TOX</td>
<td>1.505</td>
<td>m</td>
</tr>
<tr>
<td>4</td>
<td>LD</td>
<td>2.95E-07</td>
<td>m</td>
</tr>
<tr>
<td>5</td>
<td>WD</td>
<td>3.005</td>
<td>m</td>
</tr>
<tr>
<td>6</td>
<td>PHI</td>
<td>7.28</td>
<td>cm/2/V-s</td>
</tr>
<tr>
<td>7</td>
<td>VTO</td>
<td>1.23</td>
<td>V</td>
</tr>
<tr>
<td>8</td>
<td>THETA</td>
<td>0.292</td>
<td>1/V</td>
</tr>
<tr>
<td>9</td>
<td>RS</td>
<td>27.06</td>
<td>ohm</td>
</tr>
<tr>
<td>10</td>
<td>RD</td>
<td>27.06</td>
<td>ohm</td>
</tr>
<tr>
<td>11</td>
<td>DELTA</td>
<td>2.27</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>NSUB</td>
<td>1.43E+17</td>
<td>cm-3</td>
</tr>
<tr>
<td>13</td>
<td>XIC</td>
<td>1.24E-07</td>
<td>m</td>
</tr>
<tr>
<td>14</td>
<td>VMAX</td>
<td>1.03E+07</td>
<td>m/s</td>
</tr>
<tr>
<td>15</td>
<td>ETA</td>
<td>0.827</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>KAPPA</td>
<td>0.059</td>
<td>1/V</td>
</tr>
<tr>
<td>17</td>
<td>NFS</td>
<td>3.00E+11</td>
<td>cm-2</td>
</tr>
<tr>
<td>18</td>
<td>CGSO</td>
<td>3.40E-10</td>
<td>F/m</td>
</tr>
<tr>
<td>19</td>
<td>CDOS</td>
<td>3.40E-10</td>
<td>F/m</td>
</tr>
<tr>
<td>20</td>
<td>CGSO</td>
<td>3.40E-10</td>
<td>F/m</td>
</tr>
<tr>
<td>21</td>
<td>FB</td>
<td>0.92</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>XOC</td>
<td>0.80</td>
<td></td>
</tr>
</tbody>
</table>

Note: Parameters in Red come directly from SPICE Level One. Note: most parameters are 0 not 0 at end of parameter name ("sil" not "silo")

---

**Rochester Institute of Technology Microelectronic Engineering**

- **Model RITMOSFET NMOS** (LEVEL 3) TFO=1 TOX=1.55 LD=2.95 WD=3.005
- **Model RITMOSFET PMOS** (LEVEL 3) TFO=1 TOX=1.55 LD=3.16 WD=3.18
- **Other models shown below.**

---

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## PARAMETERS FOR SPICE LEVEL 49

### SPICE Parameters for BiSIM3 VER 3.1, LEVEL 49

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>Level</td>
<td>49</td>
<td>Level 9, 91, 49 or 53</td>
</tr>
<tr>
<td>Control</td>
<td>VERSION</td>
<td>3.1</td>
<td>2.0, 3.1 or 3.2 versions, default is the current version</td>
</tr>
<tr>
<td>Control</td>
<td>MOSMOD</td>
<td>1</td>
<td>Mobility model selector (1, 2, 3, 4, ... select slightly different equations for calculation of Ueff)</td>
</tr>
<tr>
<td>Control</td>
<td>CASMAX</td>
<td>2</td>
<td>Capacitance model selector (1, 2, 3, 4, ... select slightly different equations for gate capacitance)</td>
</tr>
</tbody>
</table>
| Process   | TOX                | 1.5E-08 | cm
| Process   | XI                 | 1.84E-07 | cm
| Process   | NCH                | 1.43E-12 | cm^-3
| Process   | NSUB               | 5.3E-18 | cm^-3
| Process   | XT                 | 1.43E-07 | cm
| Process   | VOS                | 5.00E+11 | cm^-2
| Process   | MINT               | 2.0E-07 | m
| Process   | LINT               | 1.43E-07 | m
| Process   | NCLIM              | 5.00 | 
| Process   | WSIDE              | 5.00E+20 | m^-3
| DiodeResistor | RSHE              | 1.092E-55 | ohm
| DiodeResistor | JS                | 3.33E-08 | Am^2
| DiodeResistor | JSW               | 3.33E-08 | Am^2
| DiodeResistor | CJ                | 6.30E-04 | PM^2
| DiodeResistor | JM                | 0.5    |
| DiodeResistor | PB                | 0.95   | V
| DiodeResistor | CFSW              | 1.265E-10 | V
| DiodeResistor | MSW               | 0.5    |
| DiodeResistor | FSW               | 0.95   | V
| AC | C0001              | 3.40E-10 | Pm^2
| AC | C0010              | 3.40E-10 | Pm^2
| AC | C0020              | 3.40E-10 | Pm^2

---

Note: All parameters use "0" at end of parameter name ("zero" not "oh")  
Note: Parameters red come directly from SPICE Level One and/or Three

---

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RESULTS USING SPICE LEVELS 49, 3, 1
go athena
# set grid
line x loc=0.0 spac=0.1
line x loc=1.0 spac=0.05
line x loc=10.0 spac=0.05
line x loc=12.0 spac=0.1
line y loc=0.0 spac=0.01
line y loc=2.2 spac=0.01
line y loc=3.5 spac=0.3
line y loc=6.0 spac=0.5

init silicon phosphor resistivity=11.3 orientation=100 space.mult=5.0

# ramp up from 800 to 900°C soak 50 min dry o2, ramp down to 800 n2
diff time=10 temp=800 t.final=900 dryo2 press=1.0 hcl.pc=0
diff time=50 temp=900 weto2 press=1.0 hcl.pc=0
diff time=20 temp=900 t.final=800 nitro press=1.0 hcl.pc=0

deposit photoresist thickness=1.0
etch photoresist left ;l.x=2.0
etch photoresist right p1.x=10.00

# ion implant drain and source
implant boron dose=1e15 energy=70 tilt=0 rotation=0 crysatal lat.ratio1=1.0 lat.ratio2=1.0

Etch photoresist all
# ramp up from 800 to 1000°C soak 90 min, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 nitro press=1.0 hcl.pc=0
diff time=90 temp=1000 nitro press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0

Starting wafer resistivity = 11.3 ohm-cm
Grow Kooi oxide 1000 Å
Ion Implant P-type D/S at Dose = 1E15
Strip photoresist
Anneal D/S implant
Ion Implant P-type channel at Dose = 0, 4e11, 1e12, 4e12

# ion implant channel
implant boron dose=4e12 energy=60 tilt=0 rotation=0 crysatal lat.ratio1=1.0 lat.ratio2=1.0

etch oxide all

# ramp up from 800 to 1000°C soak 90 min dry o2, ramp down to 800 n2
diff time=20 temp=800 t.final=1000 dryo2 press=1.0 hcl.pc=0
diff time=90 temp=1000 dryo2 press=1.0 hcl.pc=0
diff time=40 temp=1000 t.final=800 nitro press=1.0 hcl.pc=0

deposit nitride thick=0.010

Grow 700 Å gate oxide

Deposit 100 Å nitride

Temp cycle for growth of oxynitride

Deposit 100 Å oxynitride

Temp cycle for poly dope

Deposit 6000 Å poly
Deposit 5000 Å aluminum
Channel Implant Dose = 0

Crossection of MOSFET

Channel Doping Profile 1
RIT MOSFET SPICE Parameters

SILVACO ATHENA (SUPREM)

D/S Doping Profile 2

Channel Doping Profile 3

Microelectronic Engineering
SILVACO ATLAS (DEVICE SIMULATOR)

Go athena
Init infile=UofH.str

# name the electrodes...
Electrode name=gate x=6
Electrode name=source x=0
Electrode name=drain x=12
Electrode name=substrate backside

Extract name="vt" 1dvt ptype qss=1e11 workfunc=5.1 x.val=6

Go atlas

# define the gate workfunction
Contact name=gate p.poly
# define the Gate qss
Interface qf=1e11

# use the cvt mobility model for MOS
Models cvt srh

# set gate biases with Vds=0.0
Solve init
Solve vgate=0 vssubstrate=0 outf=solve_temp0
Solve vgate=-1 vssubstrate=0 outf=solve_temp1
Solve vgate=-1 vssubstrate=0 outf=solve_temp2
Solve vgate=-3 vssubstrate=0 outf=solve_temp3
Solve vgate=-4 vssubstrate=0 outf=solve_temp4
Solve vgate=-5 vssubstrate=0 outf=solve_temp5

# load in temporary file and ramp Vds
Load infile=solve_temp0
Log outf=Vg_0.log
Solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

Read in structure file created by Athena

Define location of gate, source, drain and substrate

Do calculations for given gate voltage and substrate voltage (Vg=0,-1,-2,-3,-4,-5 and Vsub=0,+5,+10+15)

Sweep drain voltage from 0 to –5 volts
In –0.5 volt steps
SILVACO ATLAS (DEVICE SIMULATOR)

# load in temporary file and ramp vds
load infile=solve_temp1
log outf=vg_1.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp2
log outf=vg_2.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp3
log outf=vg_3.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp4
log outf=vg_4.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# load in temporary file and ramp vds
load infile=solve_temp5
log outf=vg_5.log
solve name=drain vdrain=0 vfinal=-5 vstep=-0.5

# extract max current and saturation slope
extract name="pidsmax" max(abs(i."drain"))
extract name="p_sat_slope" slope(minslope(curve(abs(v."drain"), abs(i."drain"))))

@plot –overlay vg_0.log vg_1.log vg_2.log vg_3.log vg_4.log vg_5.log –setmos1ex09_1.set
quit

Sweep drain voltage from 0 to −5 volts in -0.5 volt steps
Channel Implant
Dose = none
Vsub = 0

\[ V_{gs} = -5 \]
RIT MOSFET SPICE Parameters

SILVACO ATHENA > ATLAS > UTMOST > SPICE

Extraction of SPICE Model Parameters from ATLAS
Device Simulation Using UTMOST

Many users would like to extract SPICE models from their present and device simulation using ATHENA and ATLAS to be used in actual circuit simulation without actually fabricating the device.

Using SILVACO UTMOST you can extract SPICE model parameters from the simulation results of ATHENA and ATLAS.

To guide users on how to go about extracting SPICE model parameters an example which extracts SIGMOS model from process/device simulation is used in this article.

All these commands can be executed from a single software—DeckBuild.

The comments are heavily commented so that you know their functions and purpose.

Here we will concentrate on the UTMOST batch mode commands. Here we only cover very simple case and there is no local optimization. The UTMOST interactive mode can be used once the UTMOST ramp into a file.

(UTMOST interactive cannot be executed from DeckBuild)

```plaintext
........ start of deckbuild commands ...........

# Commands that can be used in deckbuild to extract
# SPICE model Parameters. The deck for TCAD is
# not complete. Below are examples of commands that
# can be used in VHF/ATHENA and ATLAS to obtain the
# device characteristics

# Simple ATHENA/ATLAS setup
# Run process simulation

go athena
# Extract the poly length LD

extract name="14" thickness poly=0
extract name="utmost.ld""1.0e-4"

# Extract thickness oxide at occ=1 name="ox"
extract name="utmost.ox" (Box:1.0e-4)

........ start of ATLAS device simulation ........

# go atlas
```

Figure 1. TonyRee's Device Structure.
Rochester Institute of Technology
Microelectronic Engineering

ATLAS GENERATED DEVICE CHARACTERISTICS

RIT MOSFET SPICE Parameters

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NMOS PARAMETER DECK:
*2-27-2007 UTMOST EXTRCTIONS.MODEL CMOSN NMOS (LEVEL=49
VERSION=3.1 CAPMOD=2 MOBMOD=1+TOX=328.4E-10 XJ=3.5E-7 NCH=7.0E19
VTH0=0.8627+K1=0.5 K2=-0.0186 K3=80 WO=2.5E-6 NLX=1.740E-7+DVT0W=0
DVT1W=0 DVT2W=-0.032 DVT0=2.2 DVT1=0.53 DVT2=0.1394+U0=670 UA=2.25E-9
UB=5.87E-19 UC=-4.65E-11 VSAT=80000+A0=1 AGS=0 B0=0 B1=0 KETA=-0.047
A1=0 A2=1+RDSW=0 PRWG=0 PRWB=0 WR=1 WINT=2.58E-8 LINT=1.86E-8+XL=0
XW=0 DWG=0 DWB=0 VOFF=-0.06464 NFACTOR=1.3336+CIT=0 CDSC=0.00024
CDSCD=0 CDSCB=0 ETA0=0.08 ETAB=-0.07+DSUB=0.56 PCLM=1.39267
PDIBLC1=0.39 PDIBLC2=0.0086 PDIBLCB=0 +DROUT=0.19093 PSCBE1=4.00E8
PSCBE2=6E-6 PVAG=0 DELTA=0.01 PRT=0+UTE=-1.5 KT1=0 KT1L=0 KT2=0
UA1=4.3E-9 UB1=-7.6E-18+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0
WWN=1+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0+XPART=0 +CGD0=1.99E-10
CGS0=1.99E-10 CGB0=5.75E-10 CJ=4.23E-4+PB=0.99 MJ=0.4496 CJSW=3.83
PBSW=0.1083 MJSW=0.1084+PVTH0=0.02128 PRDSW=-16.155 PK2=0.0253
WKETA=0.01886 LKETA=0.0205)**
RIT MOSFET SPICE Parameters

UTMOST GENERATED SPICE PARAMETERS
FROM ATHENA SIMULATED DEVICE CHARACTERISTICS

PMOS PARAMETER DECK:
*2-27-2007 UTMOST EXTRACTIONS.MODEL CMOSP PMOS (LEVEL=49
VERSION=3.1 CAPMOD=2 MOBMOD=1+TOX=328.7E-10 XJ=3.5E-7 NCH=3.0E19
VTH0=-0.6322+K1=0.6423 K2=-0.0856046 K3=80 K3B=0 WO=2.0E-6 NLX=1.0E-
7+DVT0W=0 DVT1W=0 DVT2W=-0.032 DVT0=1.5 DVT1=0.50 DVT2=-
0.0193+U0=187.362 UA=1.1762E-9 UB=1.0E-22 UC=5.003E-3
VSAT=4.835E6+A0=3.9669 AGS=0 B0=0 B1=0 KETA=-0.0385 A1=0.19469
A2=0.40150+RDSW=0 PRWG=0 PRWB=0 WR=1 WINT=1.67E-8 LINT=3.150E-
7+XL=0 XW=0 DWG=0 DWB=0 VOFF=-0.06464 NFACTOR=1.3336+CIT=0
CDSC=0.00024 CDSCD=0 CDSCB=0 ETA0=0.08 ETAB=-0.07+DSUB=0.56
PCLM=1.39267 PDIBLC1=0 PDIBLC2=1E-5 PDIBLCCB=0 +DROUT=0.19093
PSCBE1=4E8 PSCBE2=6E-6 PVAG=0 DELTA=0.01 PRT=0+UTE=-1.5 KT1=0 KT1L=0
KT2=0 UA1=4.3E-9 UB1=-7.6E-18+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0
WWN=1+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0+XPART=0 +CGD0=2.4E-10
CGS0=2.4E-10 CGB0=5.75E-10 CJ=7.27E-4+PB=0.97 MJ=0.496 CJSW=3.115
PBSW=0.99 MJSW=0.2654+PVTH0=0.00942 PRDSW=-231.3 PK2=1.397
WKETA=1.863 LKETA=5.729)*
*1-15-2007 FROM ROB SAXER UTMOST EXTRATIONS

.Model RITSMFLN49 NMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=310E-10 XJ=9.0E-7 NCH=8.2E16 VTH0=1.026
+K1=1.724 K2=-0.1212 K3=0 K3B=0 WO=2.5E-6 NLX=4.80E-9
+DVT0W=0 DVT1W=0 DVT2W=-0.032 DVT0=0.1466 DVT1=0.038 DVT2=0.1394
+U0=687.22 UA=2.34E-9 UB=-1.85E-18 UC=-1.29E-11 VSAT=1.64E5
+A0=0.4453 AGS=0 B0=0 B1=0 KETA=-0.0569 A1=0 A2=1
+RDSW=376.9 PRWG=0 PRWB=0 WR=1 WINT=2.58E-8 LINT=1.86E-8
+XL=0 XW=0 DWG=0 DBW=0 VOFF=-0.1056 NFACTOR=0.8025
+CIT=0 CDSC=-2.59E-5 CDSCD=0 CDSCB=0 ETA0=0 ETAB=0
+DSUB=0.0117 PCLM=0.6184 PDIBLC1=0.0251 PDIBLC2=0.00202 PDIBLCB=0
+DROUT=0.0772 PSCBE1=2.77E9 PSCBE2=3.11E-8 PVAG=0 DELTA=0.01 PRT=0
+UTE=-1.5 KT1=0 KT1L=0 KT2=0 UA1=4.3E-9 UB1=-7.6E-18
+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1
+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0
+XPART=0 +CGD0=1.99E-10 CGS0=1.99E-10 CGB0=5.75E-10 CJ=4.23E-4
+PB=0.99 MJ=0.4496 CJSW=3.83 PBSW=0.1083 MJSW=0.1084
+PVTH0=0.02128 PRDSW=-16.155 PK2=0.0253 WKETA=0.01886 LKETA=0.0205)
RIT MOSFET SPICE Parameters

**UTMOST GENERATED SPICE DECK FROM MEASURED SMFL CMOS PROCESS DEVICE CHARACTERISTICS**

*1-15-2007 FROM ROB SAXER UTMOST EXTRACTIONS

MODEL RITSMFLP49 PMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=310E-10 XJ=8.8E-7 NCH=3.1E16 VTH0=-1.166
+K1=0.3029 K2=0.1055 K3=0 K3B=0 WO=2.5E-6 NLX=2.01E-8
+DVT0W=0 DVT1W=0 DVT2W=-0.032 DVT0=2 DVT1=0.5049 DVT2=-0.0193
+U0=232.53 UA=4E-9 UB=-2.26E-18 UC=-6.80E-11 VSAT=4.40E4
+A0=0.6045 AGS=0 B0=0 B1=0 KETA=-0.0385 A1=0 A2=1
+RDSW=1230 PRWG=0 PRWB=0 WR=1 WINT=1.67E-8 LINT=6.50E-8
+XL=0 XW=0 DWG=0 DWB=0 VOFF=-0.0619 NFACTOR=1.454
+CIT=0 CDSC=-4.30E-4 CDSCD=0 CDSCB=0 ETA0=0 ETAB=0
+DSUB=0.2522 PCLM=5.046 PDBLC1=0 PDBLC2=1E-5 PDBLBCB=0
+DROUT=0.2522 PSCBE1=2.8E9 PSCBE2=2.98E-8 PVAG=0 DELTA=0.01 PRT=0
+UTE=-1.5 KT1=0 KT1L=0 KT2=0 UA1=4.3E-9 UB1=-7.6E-18
+UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1
+WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0
+XPART=0 +CGD0=2.4E-10 CGS0=2.4E-10 CGB0=5.75E-10 CJ=7.27E-4
+PB=0.97 MJ=0.496 CJSW=3.115 PBSW=0.99 MJSW=0.2654
+PVTH0=0.00942 PRDSW=-231.3 PK2=1.397 WKETA=1.863 LKETA=5.729)
SMFL CMOS PROCESS “HOT & COLD” SPICE MODELS

All parameters the same except those listed are changed to give more transistor current for the hot models:

```
.model hot nmos ( LEVEL = 11     VERSION = 3.1
TOX = 2.70E-8  VTH0= 0.926   U0 = 750   RDSW = 330)
.model hot pmos ( LEVEL = 11     VERSION = 3.1
TOX = 2.70E-8  VTH0= -1.066  U0 = 250   RDSW = 1.00E3)

.model cold nmos ( LEVEL = 11     VERSION = 3.1
TOX = 3.50E-8  VTH0= 1.126   U0 = 620   RDSW = 410)
.model cold pmos ( LEVEL = 11     VERSION = 3.1
TOX = 3.50E-8  VTH0= -1.266  U0 = 200   RDSW = 1.45E3)
```
REFERENCES


7. ICCAP Manual, Hewlet Packard
1. Write an abstract that summarizes the main ideas presented in this document.