

# Introduction to Modeling MOSFETS in SPICE

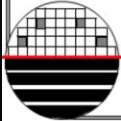
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Dept Webpage: <http://www.rit.edu/kgcoe/microelectronic/>



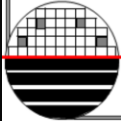
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2-6-2019 SPICE\_MOSFET\_Model\_Intro.ppt

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## ADOBE PRESENTER

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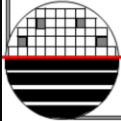


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No notes

## OUTLINE

Introduction  
MOSFET  
SPICE  
Shichman and Hodges Model  
MOSFET Attributes  
Changing MOSFET SPICE Model  
Ids-Vds Family of Curves  
Ids-Vgs  
Measured MOSFET Characteristics  
AC Attributes  
Ring Oscillator  
Summary  
References  
Homework



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Outline

## *INTRODUCTION*

PSpice Lite 9.2 is one of the OrCAD family of products, from Cadence Design Systems, Inc., offering a complete suite of electronic design tools. It is free and includes limited versions of OrCAD Capture, for schematic capture, PSpice for analog circuit simulation and Pspice A/D for mixed analog and digital circuit simulation. PSpice Lite 9.2 is limited to 64 nodes, 10 transistors, two operational amplifiers and 65 primitive digital devices. See page 35 (xxxv) of the PSpice Users Guide.

LT SPICE – is a free SPICE simulator with schematic capture from Linear Technology. It is quite similar to PSpice Lite but is not limited in the number of devices or nodes. Linear Technology (LT) is one of the industry leaders in analog and digital integrated circuits. Linear Technology provides a complete set of SPICE models for LT components.

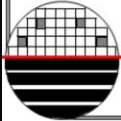
Pspice Lite and LT SPICE are the popular free version of SPICE with schematic capture.



## **MOSFET DEVICE MODELS**

MOSFET Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, Level 7, Level 8, Level 49, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.

In general first generation models are recommended for MOSFETs with gate lengths of 10 $\mu$ m or more. If not specified most SPICE MOSFET Models default to level=1 (Shichman and Hodges)

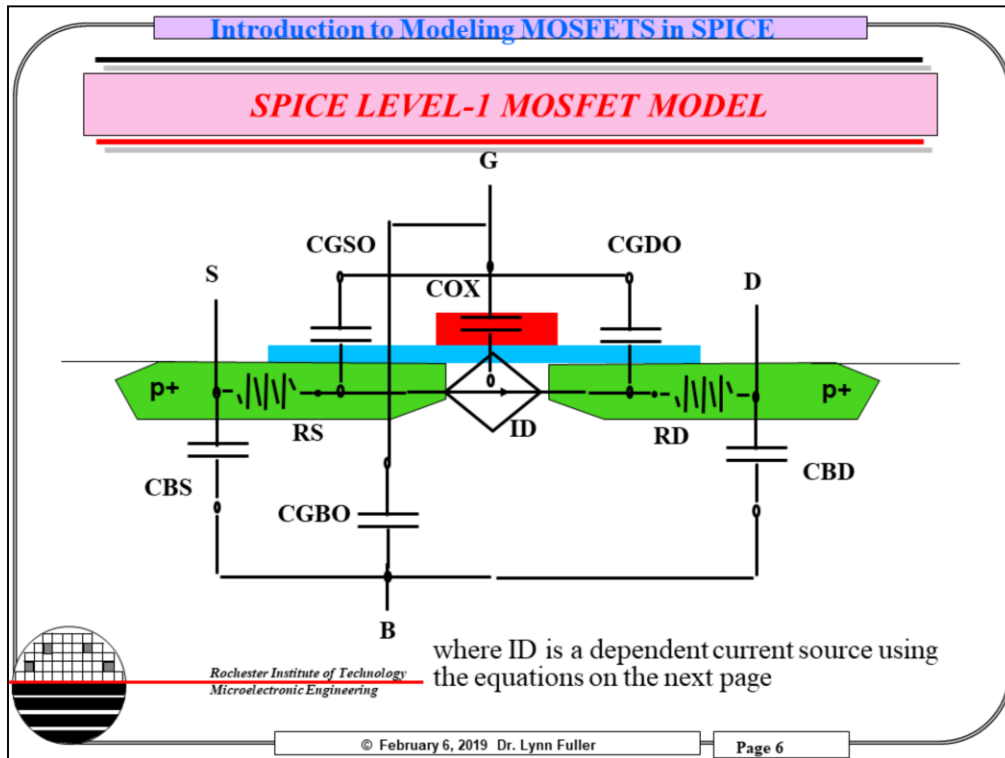


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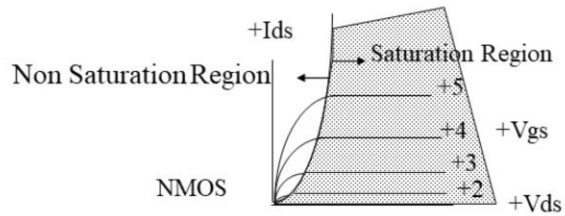
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Please Read



This schematic shows the components in a MOSFET model. The internal resistors and capacitors and the dependent current source ID.

**SPICE LEVEL 1 - SHICHMAN AND HODGES**

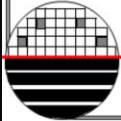


$$I_{Dsat} = \frac{\mu W C_{ox'}}{2L} (V_g - V_t)^2$$

Saturation Region

$$I_D = \frac{\mu W C_{ox'}}{L} (V_g - V_t - V_d/2) V_d$$

Non Saturation Region



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where  $\mu$ ,  $C_{ox'}$  and  $V_t$  are given in equations on the next pages

These are the equations for current  $I_D$  in the saturation and non saturation regions of operation.

**SPICE LEVEL-1 EQUATIONS FOR  $\mu_0$ ,  $V_{TO}$  AND  $C_{OX}$**

Mobility:  
(cm<sup>2</sup>/V-s)

$$\mu = \mu_{min} + \frac{(\mu_{max} - \mu_{min})}{\{1 + (N/N_{ref})^\alpha\}}$$

Parameter	Arsenic	Phosphorous	Boron
$\mu_{min}$	52.2	68.5	44.9
$\mu_{max}$	1417	1414	470.5
$N_{ref}$	$9.68 \times 10^{16}$	$9.20 \times 10^{16}$	$2.23 \times 10^{17}$
$\alpha$	0.680	0.711	0.719

Threshold Voltage:  
+/-  
nmos/pmos

$$V_{TO} = \Phi_{ms} - q \text{NSS}/C_{ox}' + /-2[\Phi_F] + /-2(q\epsilon_0\epsilon_{rsi} \text{NSUB} [\Phi_F])^{0.5}/C_{ox}'$$

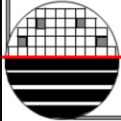
$$[\Phi_F] = (KT/q) \ln (\text{NSUB}/n_i) \quad \text{where } n_i = 1.45 \times 10^{10} \text{ and } KT/q = 0.026$$

Absolute value

Gate Capacitance  
per unit area  $C_{ox}'$

$$C_{ox}' = \epsilon_{rox} \epsilon_0 / TOX = 3.9 \epsilon_0 / TOX$$

$$\Phi_F = 2 [\Phi_F]$$



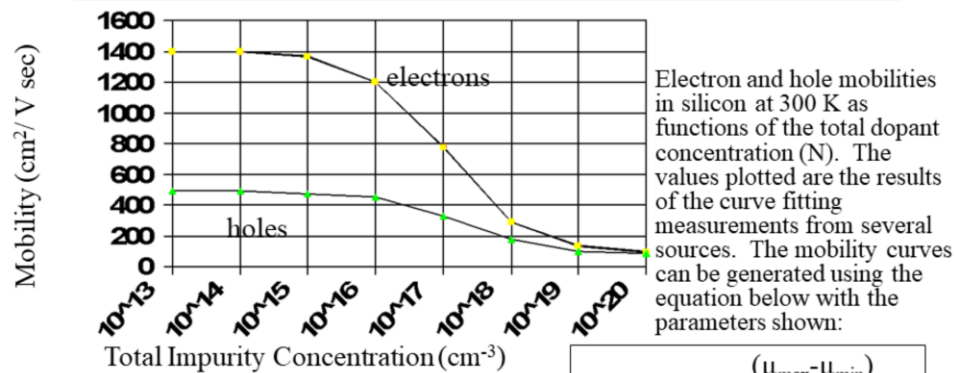
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where  $\epsilon_{rsi} = 11.7$  and  $\epsilon_{rox} = 3.9$

$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$  or  $8.8 \times 10^{-14} \text{ F/cm}$

$q = 1.6 \times 10^{-19}$

These equations are the basic Level 1 models for mobility, threshold voltage and gate oxide capacitance per unit area.

**MOBILITY MODEL**

$$\mu(N) = \mu_{mi} + \frac{(\mu_{max} - \mu_{min})}{\{1 + (N/N_{ref})^\alpha\}}$$

From Muller and Kamins, 3<sup>rd</sup> Ed., pg 33

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Parameter	Arsenic	Phosphorous	Boron
$\mu_{min}$	52.2	68.5	44.9
$\mu_{max}$	1417	1414	470.5
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$\alpha$	0.680	0.711	0.719

Mobility is shown here as a function of total doping concentration. Mobility is also a function of temperature, electric field, strain and other parameters. More complex mobility models are available for advanced MOSFET SPICE analysis.

## LONG CHANNEL THRESHOLD VOLTAGE, $V_T$

$$\text{Flat-band Voltage } V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C'_{ox}} - \frac{1}{C'_{ox}} \int_0^{X_{ox}} \frac{X}{X_{ox}} \rho(x) dx$$

p-type substrate (n-channel)                      n-type substrate (p-channel)                       $Q_{ss} = q N_{ss}$

$$\text{Bulk Potential: } \phi_p = -KT/q \ln(N_A/n_i)$$

$$\phi_n = +KT/q \ln(N_D/n_i)$$

$$\text{Work Function Difference: } \phi_{MS} = \phi_M - (X + Eg/2q + [\phi_p])$$

$$\phi_{MS} = \phi_M - (X + Eg/2q - [\phi_n])$$

**\*Maximum Depletion Width:**

$$\sqrt{\frac{4 \epsilon_s [\phi_p]}{q N_A}}$$

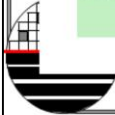
$$\sqrt{\frac{4 \epsilon_s [\phi_n]}{q N_D}}$$

$$\text{NMOS Threshold Voltage: } V_T = V_{FB} + 2 [\phi_p] + \frac{1}{C'_{ox}} \sqrt{2 \epsilon_s q N_A (2 [\phi_p])}$$

p-type substrate

$$\text{PMOS Threshold Voltage: } V_T = V_{FB} - 2 [\phi_n] - \frac{1}{C'_{ox}} \sqrt{2 \epsilon_s q N_D (2 [\phi_n])}$$

n-type substrate



These are the equations for MOSFET threshold voltage. The flat band voltage would be zero if the gate material and the semiconductor material had the same work function and the value of  $Q_{ss}$  (surface state density) was zero and no trapped charge in the oxide ( $\rho(x)$ ) in the third term. The work function is a material property and in semiconductors also depends on the doping concentration. If the gate was n-type poly and the FET was p-type (n-well) and the doping of the n-type poly was equal to the doping at the surface of the n-well was the same then the  $\phi_{MS}$  would be zero. Typically  $\phi_{MS}$  is not zero.  $Q_{ss}$  is always positive because that charge comes from surface states created by the loss of electrons from some silicon atoms at the surface because silicon dioxide can not covalently bond with all the silicon atoms available and thus some electrons migrate away from the surface leaving a positive surface charge. The second term in the equation for threshold voltage is  $2 \phi$  which is the semiconductor potential at threshold voltage where the surface is inverted to a concentration equal in magnitude to the concentration in the bulk. The last term is a voltage  $Q$  over  $C'_{ox}$  that depends on the doping concentration at the surface, assuming source and substrate are at the same voltage. Similar to the semiconductor built-in voltage plus reverse bias voltage in a uniformly doped pn junction ( $\sim 0.7 + V_R$ ). The body effect comes from this  $V_R$ .

**DISCUSSION OF MOSFET  $V_T$  EQUATIONS**

These are the equations for MOSFET threshold voltage. The flat band voltage would be zero if the gate material and the semiconductor material had the same work function and the value of  $Q_{ss}$  (surface state density) was zero and no trapped charge in the oxide ( $Rho(x)$ ) in the third term. The work function is a material property and in semiconductors also depends on the doping concentration. If the gate was n-type poly and the FET was p-type (n-well) and the doping of the n-type poly was equal to the doping at the surface of the n-well was the same then the  $\Phi_{MS}$  would be zero. Typically  $\Phi_{MS}$  is not zero.  $Q_{ss}$  is always positive because that charge comes from surface states created by the loss of electrons from some silicon atoms at the surface because silicon dioxide can not covalently bond with all the silicon atoms available and thus some electrons migrate away from the surface leaving a positive surface charge. The second term in the equation for threshold voltage is  $2\Phi$  which is the semiconductor potential at threshold voltage where the surface is inverted to a concentration equal in magnitude to the concentration in the bulk. The last term is a voltage  $Q/C'_{ox}$  that depends on the doping concentration at the surface, assuming source and substrate are at the same voltage. Similar to the semiconductor built-in voltage plus reverse bias voltage in a uniformly doped pn junction ( $\sim -0.7 + V_R$ ). The body effect comes from this term.



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**BACK-BIASING EFFECTS – GAMMA**

**Body Effect coefficient GAMMA or  $\gamma$ :**

$I_{ds}$

$V_{sb}=0$   $V_{sb}=1V$   $V_{sb}=2V$

$V_{TO}$   $V_{gs}$

$V_{sb}$   $V_b$   $V_s$   $V_g$   $V_d$

p n n

$$\gamma = \frac{1}{C_{ox}'} \sqrt{2q\epsilon_{si}N_{sub}}$$

$$V_T = \Phi_{MS} - \frac{Q_{ss}}{C_{ox}'} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}}$$

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where  $\epsilon_{rsi} = 11.7$  and  $\epsilon_{rox} = 3.9$   
 $\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$   
 $q = 1.6 \times 10^{-19}$

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Body effect coefficient Gamma comes from the equations for threshold voltage on the previous page. It is a function of gate oxide thickness TOX and substrate doping NSUB. The body effect causes a shift in the threshold voltage for non zero voltages from source to substrate. VSB is positive for NMOSFETs.



***VT ADJUST IMPLANT***

The threshold voltage can be adjusted with an ion implant. If total implant dose is shallow (within  $W_{dmax}$ ) then the change in  $V_t$  is:

$$\pm \Delta V_t = q \text{ Dose}^* / C_{ox}'$$

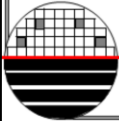
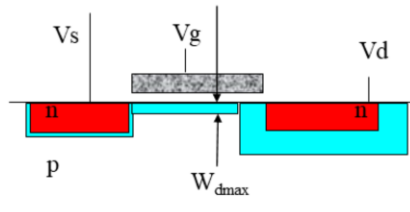
where  $\text{Dose}^*$  is the dose that is added to the Si  
 $C_{ox}'$  is gate oxide capacitance/cm<sup>2</sup>  
 $C_{ox}' = \epsilon_0 \epsilon_r / X_{ox}$

Boron gives + shift

Phosphorous gives - shift

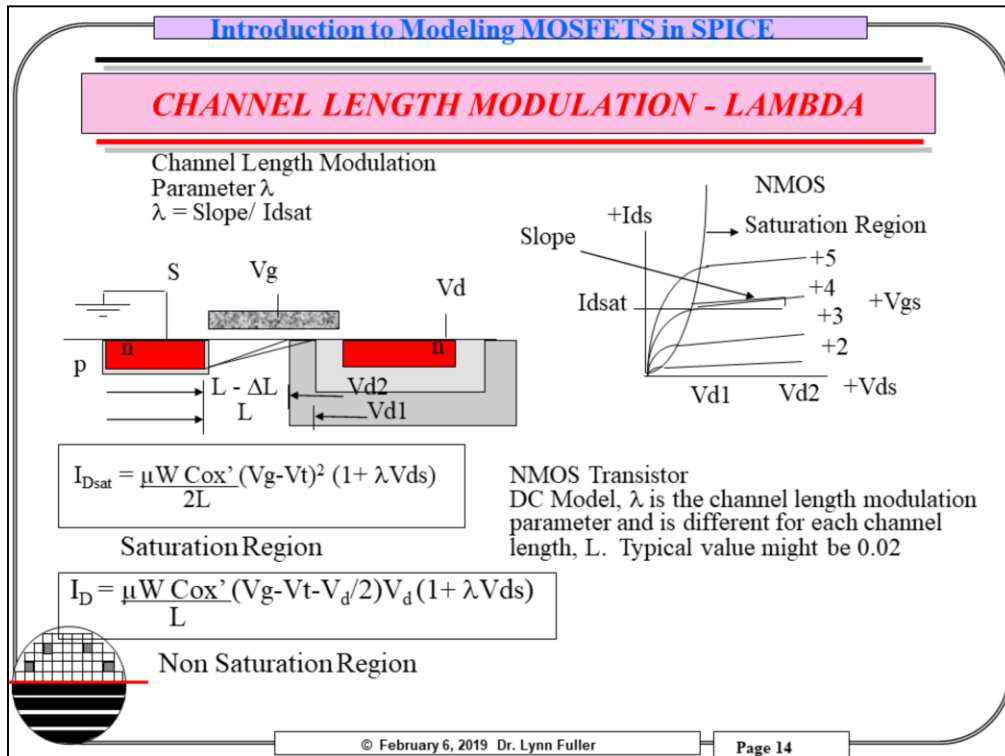
Maximum Depletion Width:

$$W_{dmax} = \sqrt{\frac{4 \epsilon_s [\phi_p]}{qN}}$$



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When using ion implant to adjust the threshold voltage of a transistor. The implant needs to be shallow enough so that all the implanted ions are in the depletion region under the gate. The shift is given in the equation in the box. Boron gives a positive shift. Phosphorous gives a negative shift. If a threshold adjust implant exists SPICE does not calculate the effect on  $V_{TO}$ . (enter  $V_{TO}$  as a SPICE model parameter rather than letting SPICE calculate  $V_{TO}$  from  $TOX$ ,  $NSS$ ,  $NSUB$  and type of gate)



Channel length modulation is a result of the change in the drain space charge layer as a function of the reverse bias voltage of the drain to substrate junction. As the drain voltage increases the space charge layer increases making the effective channel length shorter. Thus the charge transit time is shorter resulting in an increase in current. The parameter Lambda in the  $(1 + \lambda V_{\text{ds}})$  expression models this increase in current.

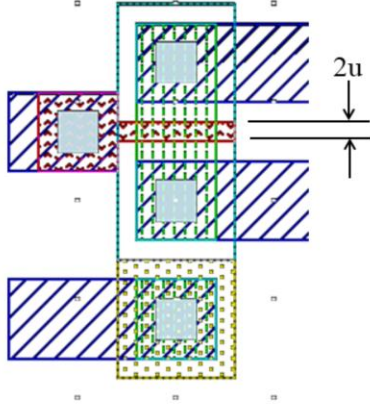
The  $(1 + \lambda V_{\text{ds}})$  term in both equations model the increase in  $I_{\text{d}}$  as  $V_{\text{ds}}$  increases seen as slope in the saturation region. (but also increases  $I_{\text{d}}$  in the non saturation region)

Introduction to Modeling MOSFETS in SPICE

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TRANSISTOR PROPERTIES OR ATTRIBUTES

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$$L = 2u$$

$$W = 8u$$

$$A_d = 8u \times 10u = 80p$$

$$A_s = A_d = 80p$$

$$P_d = 8u + 10u + 8u + 10u = 36u$$


$$P_s = P_d = 36u$$

$$N_{rs} = 1$$

$$N_{rd} = 1$$

NMOS 2/8

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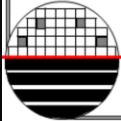
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Properties such as Length, Width, Area of Drain, Area of Source, Perimeter of Drain, Perimeter of Source, Number of squares between drain contact and channel, number of squares between source contact and channel and other attributes such as package type, etc. are also given for each transistor. These properties are combined with SPICE model parameters to give values for internal capacitors, internal resistors, etc.

### ***LTSPICE MOSFET ATTRIBUTES***

MOSFETS are four terminal devices (Drain, Gate, Source and Substrate).  $L$  and  $W$  are channel length and width in meters,  $A_d$  and  $A_s$  are area of drain and source in square meters. If not specified default values are used. (see next page) Perimeter of Drain and source ( $PD$  and  $PS$ ) in meters is used to calculate drain and source side wall capacitance. If  $PD$  and  $PS$  are not given the default is zero.  $NRD$  and  $NRS$  are multiplied by the drain and source sheet resistance to give series resistance  $R_D$  and  $R_S$ . The default value for  $NRD$  and  $NRS$  is one.



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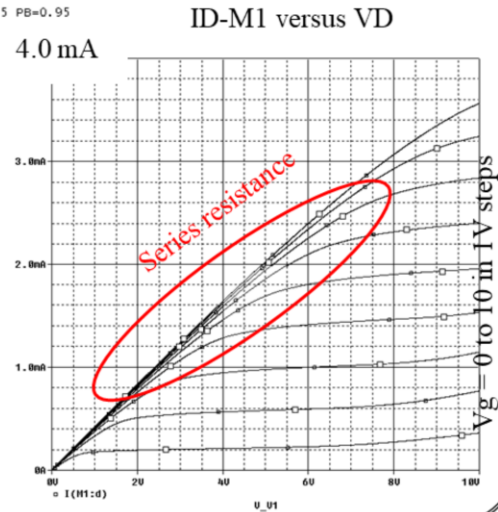
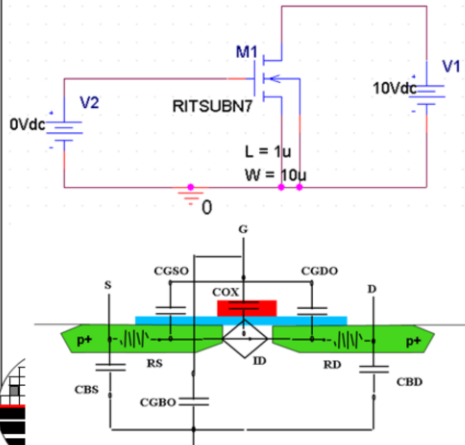
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MOSFET attributes

## EFFECT OF SERIES RESISTANCE

```
* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1.082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 NDSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGB0=5.75E-10)
*
```



## EFFECT OF SERIES RESISTANCE

```
*
* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
```

Series resistance  $R_d$  and  $R_s$

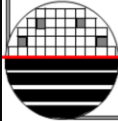
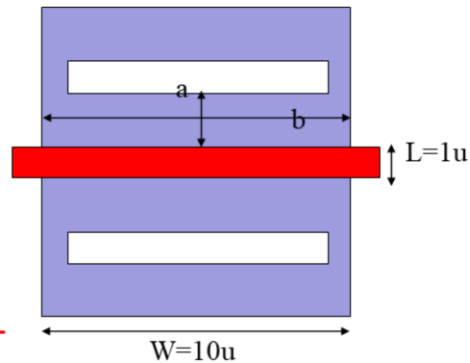
$$R_d = R_s = \text{NRD} \times \text{RSH}$$

NRD is a property =  $a/b$

RSH is a SPICE parameter

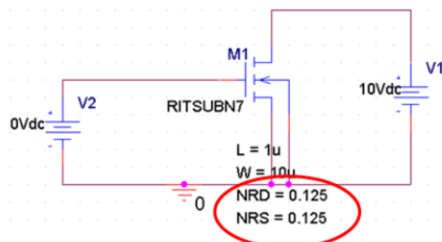
Note: if  $a=b$  then  $\text{NRD} = a/b = 1$

if  $a=1\mu$  and  $b=10\mu$  then  $\text{NRD} = 0.1$

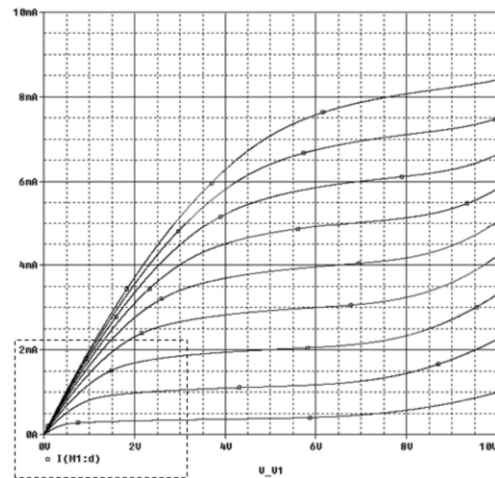


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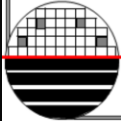
## GETTING SERIES RESISTANCE RIGHT



Note: LTSPICE and PSPICE have typical default value for NRD = NRS of one. It is best not to use the default value.



Also the voltages used change appearance (slopes) of curves. (LAMBDA does not model this)



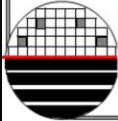
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**LTSPICE MOSFET ATTRIBUTE DEFAULT VALUES**

Name	Description	Unit	Default	Example
L	Default Length	m	defl	100u
W	Default Width	m	defw	100u
Ad	Default drain area	m2	defad	1000p
As	Default source area	m2	defas	1000p
Pd	Default drain perimeter	m	0	200u
Ps	Default source perimeter	m	0	200u
Nrd	Default drain squares	-	1	1
Nrs	Default source squares	-	1	1
Nrg	Default gate squares	-	0	1
Nrb	Default bulk squares	-	0	1
Lmin	Bin length lower limit	m	0	10u
Lmax	Bin length upper limit	m	0	20u
Wmin	Bin width lower limit	m	0	10u
Wmax	Bin width upper limit	m	0	20u



Some of the attributes for a MOSFET are shown here.

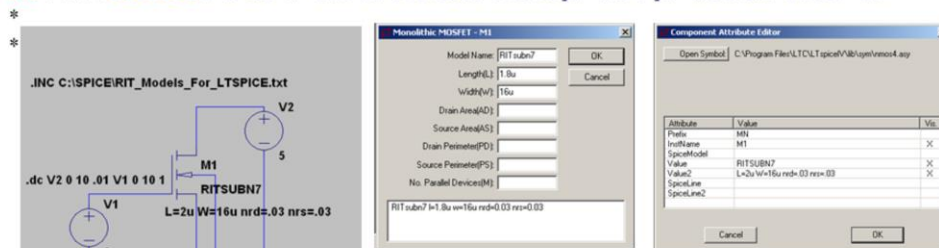


## MOSFET DEFINITION - LTSPICE

### For example:

- \* SPICE Input File
- \* MOSFET names start with M.... **M1** is the name for the MOSFET below and its drain, gate, source and substrate is connected to nodes 3,2,0,0 respectively. The model name is **RITSUBN7**.
- \* The parameters/attributes is everything after that.

**M1** 3 2 0 0 **RITSUBN7** L=2U W=16U ad=96e-12 as=96e-12 pd=44e-6 ps=44e-6 nrd=1.0 nrs=1.0



LTSPICE schematic showing **.Include** and **.dc** sweep commands. Properties dialog box to define L and W values. Note: attributes with no entry field **nrs** and **nrd** are typed in bottom box. Attribute Editor (CTRL R-click on the transistor) allows attributes with Vis.=X to be displayed on the schematic.

MOSFET M1 is defined by the RITSUBN7 SPICE model located as given in the .Include statement on the schematic and the attributes (or properties) shown in the attribute editor dialog box.

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**MOSFET DEFINITION - PSPICE**

**For example:**

- \* SPICE Input File
- MOSFET names start with M.... **M1** is the name for the
- MOSFET below and its drain, gate, source
- and substrate is connected to nodes 3,2,0,0 respectively.
- The model name is **RITSUBN7**.
- \* The parameters/attributes is everything after that.

**M1** 3 2 0 0 **RITSUBN7** L=2U W=16U ad=96e-12 as=96e-12  
+pd=44e-6 ps=44e-6 nrd=1.0 nrs=1.0

\*  
\*

In PSPICE the Attribute Editor (R-click on the transistor and edit properties) allows attributes values to be set, new attribute columns to be created, and attributes can be selected to be displayed on the schematic..

A	
SCHEMATIC1: PAGE1	
AD	
AS	
Color	Default
Designator	
Graphic	MbreakN Normal
ID	
Implementation	MbreakN
Implementation Path	
Implementation Type	PSPICE Model
L	2u
Location X-Coordinate	450
Location Y-Coordinate	270
M	
Name	INS30
NRB	
NRD	
NRG	
NRS	
Part Reference	M1
PCB Footprint	
PD	
Power Pins Visible	<input type="checkbox"/>
Primitive	DEFAULT
PS	
PSPICE Only	TRUE
PSPICE Template	M*@REFDES %d %g %s %
Reference	M1
Source Library	C:\CADENCE\SPB_16
Source Package	MbreakN
Source Part	MbreakN Normal
Value	MbreakN
W	16u

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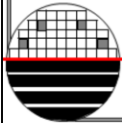
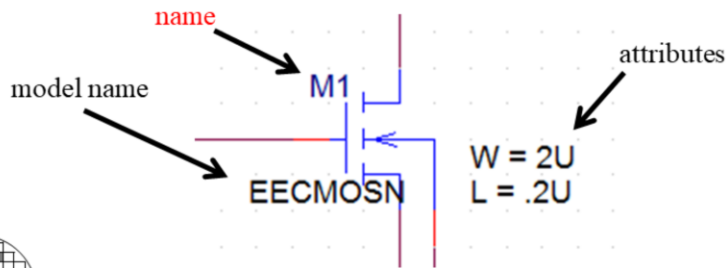
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Page 22

This is the attribute editor in PSPICE. Attributes include L, W, Ad, As, Pd, Ps, etc. PSPICE also has attributes such as package type and other properties used with other Cadence software such as circuit board layout.

**MOSFET DEFINITION - PSPICE**

In SPICE a transistor is defined by its **name** and associated **properties or attributes** and its **model**. MOSFET names start with M, attributes (L, W, Ad, As, etc.) are specified by the user and shown in the input file net list. Some attributes can be displayed on the schematic. The model is specified in a file in a given location or is defined in a library.



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Attributes can be selected to be displayed on the schematic by clicking on an attribute, display and apply in the attribute editor. Changing the model name should change the implementation value otherwise change it in the attribute editor.

## ***CHANGING THE MOSFET SPICE MODEL IN LTSPICE***

There are several ways to change the MOSFET SPICE model. A good way to do it is to create a text file on your computer and put your models in that text file and save it in some folder. You can copy models from Dr. Fuller's webpage to start your collection of models.

See: <http://people.rit.edu/lffeee/CMOS.htm>

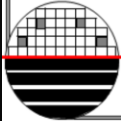
Example contents of that file is shown on the page below.

Next you change the model name for your transistor by right-click on the model name shown in your schematic and typing the model name used in the model file. (for example: RITSUBN7)

Finally you place a SPICE directive on your schematic by clicking on the .op icon on the top banner and type the following command:

`.include Drive:\path\folder\filename`

For example `.include C:\SPICE\RIT_Models_For_LTSPICE.txt`

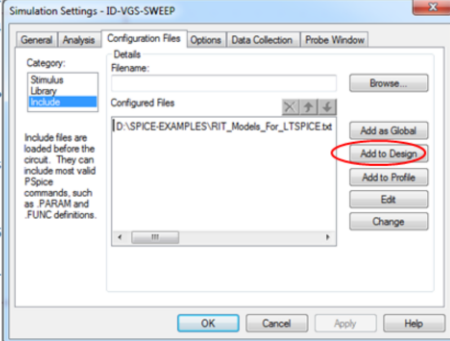


Please Read

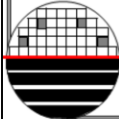
## CHANGING THE MOSFET SPICE MODEL IN PSPICE

```

*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=170u Ad=8500p As=8500p Pd=440u Ps=4
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=4E-8 XJ=2.9E-7 NCH=4E15 NSUB=5.33E15 XT=8.66E-8
+VTH0=1.4 U0= 1300 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=300 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-8 MJ=0.5 P
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=360u Ad=18000p As=18000p Pd=820u Ps
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-8 XJ=2.26E-7 NCH=1E15 NSUB=8E14 XT=8.66E-8
+VTH0=-1.65 U0= 400 WINT=1.0E-6 LINT=1E-6
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-8 MJ=0.5
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
        
```



In PSPICE models saved in a text file can be included as a configuration file in the Simulation Settings dialog box as shown above. Change the component model name to the model name in the text file.



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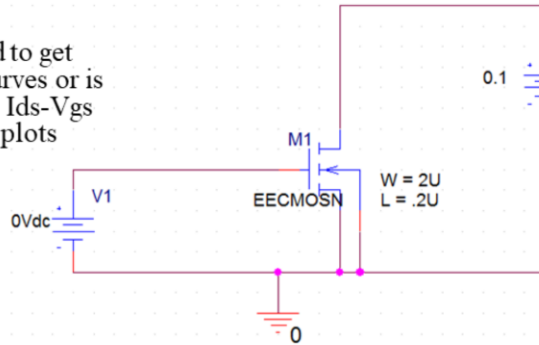
Page 25

If you want to use your own MOSFET SPICE models just create a text file and store it in some location on your computer. Then link that file (Add to Design) to the schematic in the Simulation Settings dialog box as shown.

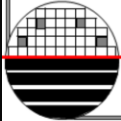
**COMPARISON OF MOSFET CHARACTERISTICS**

The circuit shown can be used to see the transistor family of  $I_{ds}$ - $V_{ds}$  curves,  $I_{ds}$ - $V_{gs}$  plot and  $I_{ds}$ - $V_{gs}$  ( $I_{ds}$  on log scale) Subthreshold plot. We can investigate the effect of changing attributes, SPICE model and model parameters.

V1 is stepped to get family of curves or is swept to get  $I_{ds}$ - $V_{gs}$  and Sub- $V_t$  plots



V2 is swept to get family of curves or is held constant to get  $I_{ds}$ - $V_{gs}$  plots



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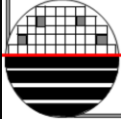
This circuit can be used to simulate transistor characteristics including  $I_d$ - $V_{ds}$ ,  $I_d$ - $V_{gs}$ , and LOG  $I_d$  vs.  $V_{gs}$ .

## MOSFET MODELS USED BY LTSPICE

LTSPICE uses several different types of MOSFET models including simple, deep submicrometer, Silicon On Insulator (SOI), Vertical double diffused Power MOSFET. Level = 1 is the default if a model level is not specified.

Level

- |          |  |   |                                   |
|----------|--|---|-----------------------------------|
| 1        | Shichman and Hodges                                      | } | 1 <sup>st</sup> generation models |
| 2        | MOS2, Vladimirescu and Liu, UC Berkeley, October 1980    |   |                                   |
| 3        | MOS3, a semi-empirical model, UC Berkeley                |   |                                   |
| 4        | BSIM UC Berkeley, May 1985                               | } | 2 <sup>nd</sup> generation models |
| 5        | BSIM2, UC Berkeley, October 1990                         |   |                                   |
| 6        | MOS6, UC Berkeley, March 1990                            |   |                                   |
| 8        | BSIM3V3.3.0, UC Berkeley 2005                            | } | 3 <sup>rd</sup> generation models |
| 9        | BSIMSOI3.2, Silicon on Insulator (SOI), UC Berkeley 2004 |   |                                   |
| 14       | BSIM4.6.1, UC Berkeley 2007                              |   |                                   |
| more.... |  |   |                                   |



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MOSFET models used by LTSPICE.

### THREE DIFFERENT NMOS SPICE MODELS

\* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology  
 .MODEL RITSUBN7 NMOS (LEVEL=7  
 +VERSION=3.1 CAPMOD=2 MOBMOD=1  
 +TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8  
 +VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7  
 +NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95  
 +CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5  
 +CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)  
 \*

\* From Electronics II EEEE482 FOR ~100nm Technology - Deep Sub-Micron  
 .model EECMOSN NMOS (LEVEL=7  
 +VERSION=3.1 CAPMOD=2 MOBMOD=1  
 +TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8  
 +VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8  
 +NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95  
 +CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5  
 +CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)  
 \*

\* From Electronics II EEEE482 SIMPLE MODEL using textbook equations  
 .model EENMOSNMOS (VTO=0.4 KP=432E-6 GAMMA=0.2 PHI=.88)

These are the spice models used.



**Introduction to Modeling MOSFETS in SPICE**

**PSPICE MOSFET MODEL PARAMETERS**

95 mosfet model parameters used by  
cadence PSPICE for **Level 7** BSIM

Start Page	File	Page 1
0001	LEVEL	8
0002	L	100.000000E-06
0003	W	100.000000E-06
0004	VTO	-4
0005	KF	414.377300E-06
0006	GAMMA	0
0007	PHI	
0008	LAMBDA	0
0009	RSN	1.000000E+03
0010	IS	1.000000E-15
0011	JS	35.100000E-09
0012	JSSN	35.100000E-09
0013	FB	.94
0014	FSN	.94
0015	CJ	528.000000E-06
0016	CJZW	119.000000E-12
0017	MJTN	.5
0018	CGSO	450.000000E-12
0019	CGDO	450.000000E-12
0020	CGBO	575.000000E-12
0021	NSUB	50.000000E+15
0022	TOX	5.000000E-09
0023	XJ	50.000000E-09
0024	UCRIT	10.000000E+03
0025	DIGNOC	1
0026	VFB	-1
0027	LETA	0
0028	NETA	0
0029	VO	100
0030	TEMP	
0031	VDC	
0032	XIPART	0
0033	VTR0	-4
0034	UA	1.000000E-09
0035	UB	100.000000E-21
0036	UC	46.500000E-12
0037	VJAT	80.000000E+03
0038	RSN	200
0039	VOFF	-.08
0040	PCIM	5
0041	AO	1
0042	A1	0
0043	A2	1
0044	WFEAR	100.000000E+15

31 mosfet model parameters used by cadence PSPICE for  
**Level 1** Shichman and Hodges

File	Page 1	ID-VGS-ON	SCHEMATIC	ID-VGS-S
LEVEL	1			
L	100.000000E-06	100.000000E-06		
W	100.000000E-06	100.000000E-06		
VTC	-4	-4		
KF	432.000000E-06	122.000000E-06		
GAMMA	.2	.2		
PHI	.68	.68		
LAMBDA	0	0		
RSN	10.000000E-15	10.000000E-15		
JS	0	0		
JSSN	.8	.8		
FB	.8	.8		
FSN	0	0		
CJ	0	0		
CJZW	0	0		
CGSO	0	0		
CGDO	0	0		
CGBO	0	0		
NSUB	0	0		
TOX	0	0		
UCRIT	10.000000E+03	10.000000E+03		
DIGNOC	1	1		
LETA	0	0		
NETA	0	0		
VO	0	0		
TEMP	0	0		
VDC	5	5		
XIPART	0	0		

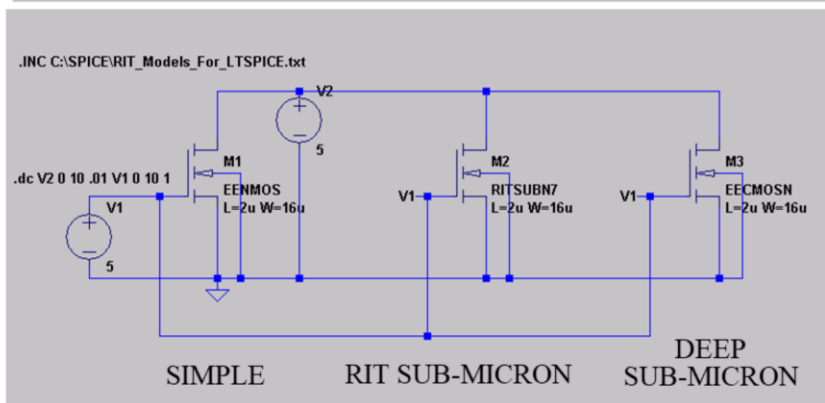
[View Output File](#)

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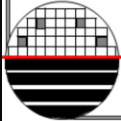
Page 29

To see the MOSFET SPICE parameters used in a simulation select view output file and scroll to the bottom. Note both level 1 and level 8 show default values of L and W at 100um. These are overridden if L and W are specified by the user.

## LTSPICE CIRCUIT SCHEMATIC



Three transistor all the same L=2u and W=16u but with different SPICE models. (SIMPLE, RIT SUB-MICRON and 100nm DEEP SUB-MICRON

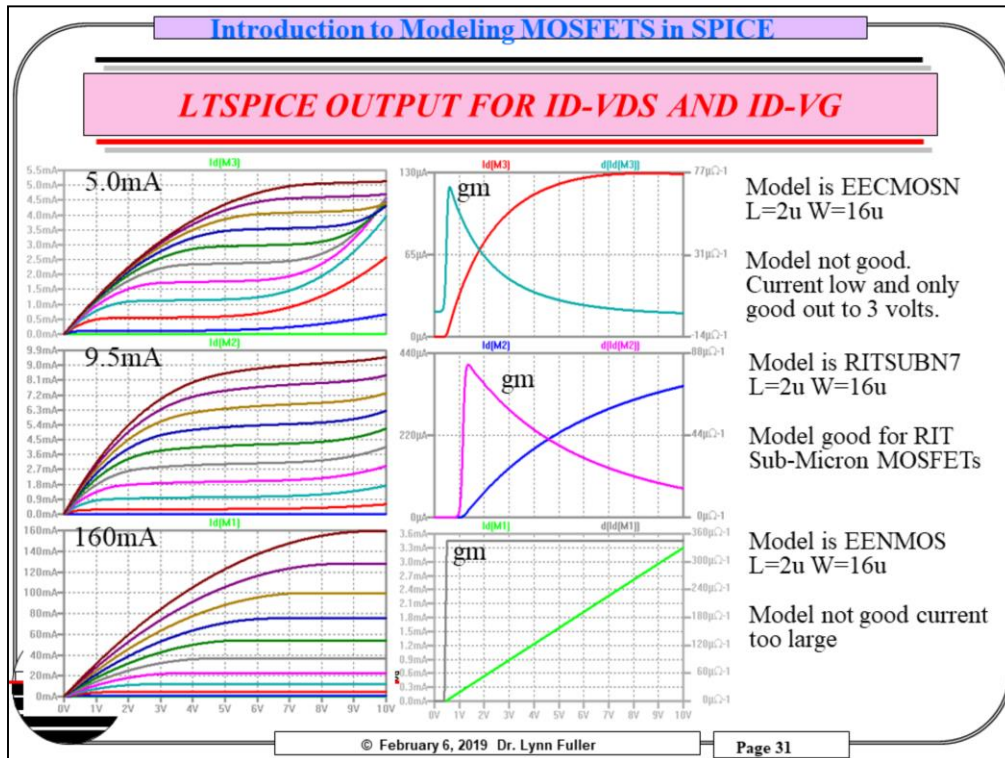


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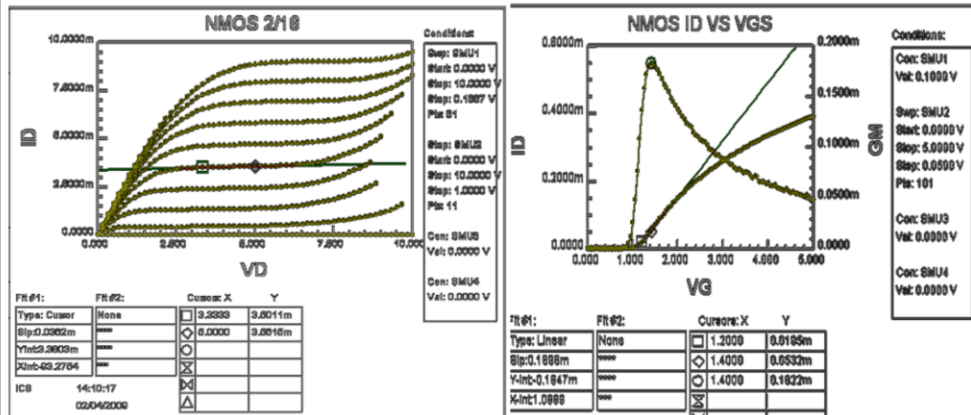
Page 30

This circuit is used to investigate the transistor characteristics for different SPICE models.

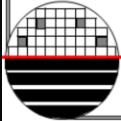


This is the simulated  $I_D$ - $V_{DS}$  family of  $V_{GS}$  curves and the  $I_D$ - $V_{GS}$  and  $g_m = d(I_D)/dV_{GS}$  curve. The three different models give very different results.

## MEASURED MOSFET ID-VDS AND ID-VGS

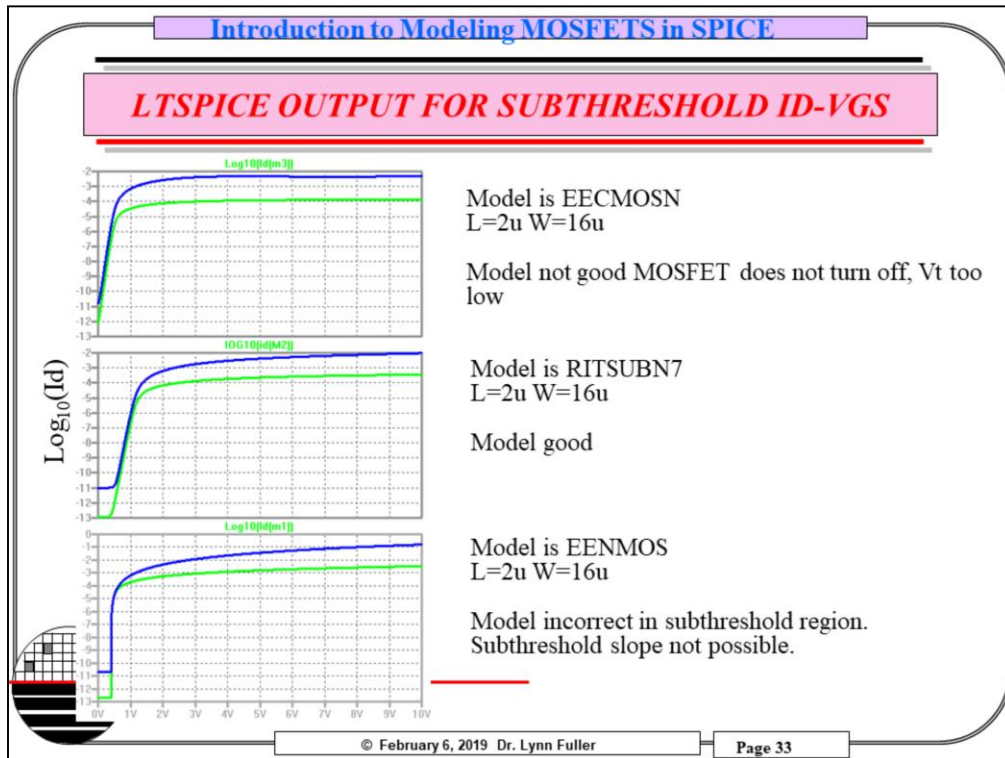


$I_{max} = 9.5mA$

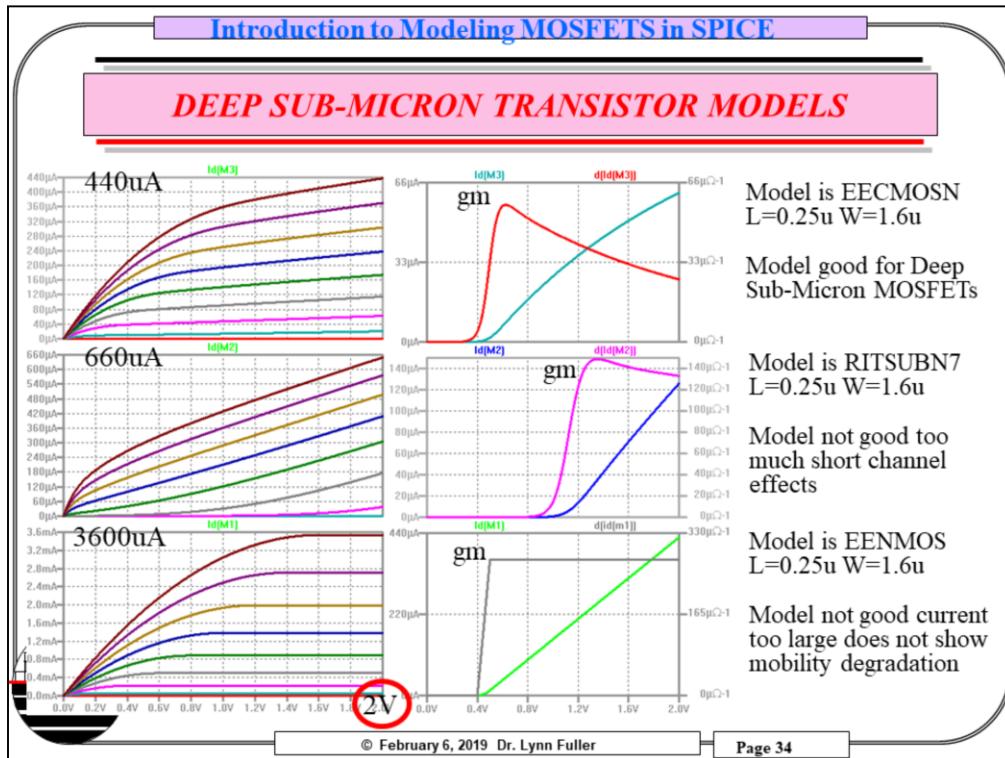


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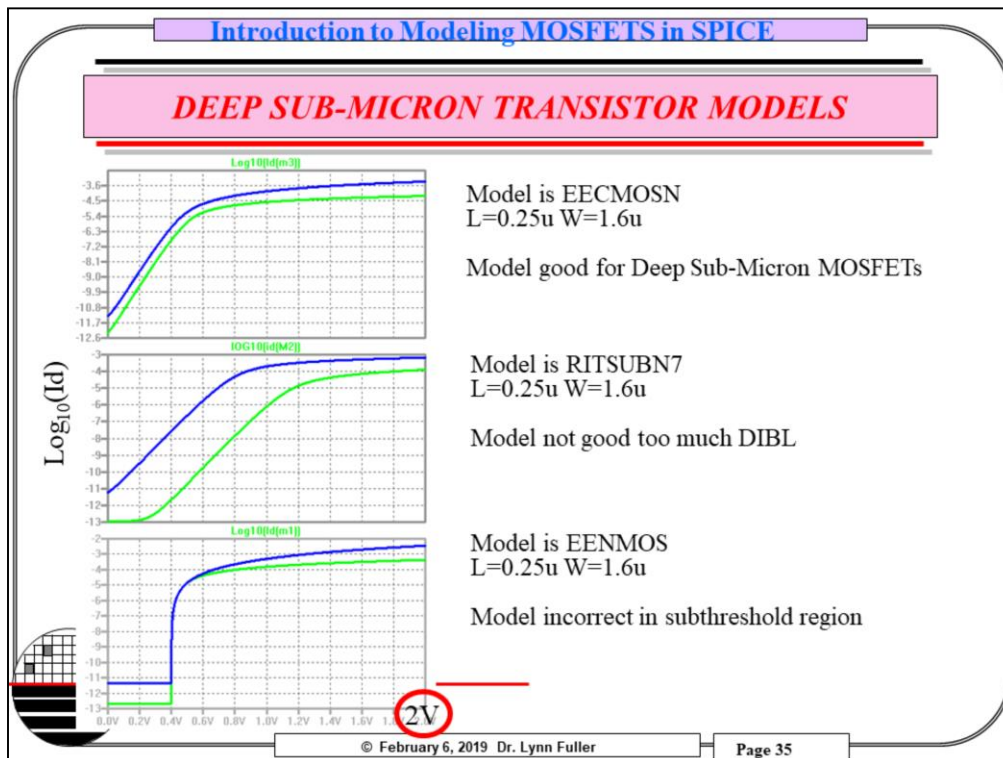
Comparing the measured results to the simulated results shows which models should be used.



Comparison of sub threshold characteristics using different models.

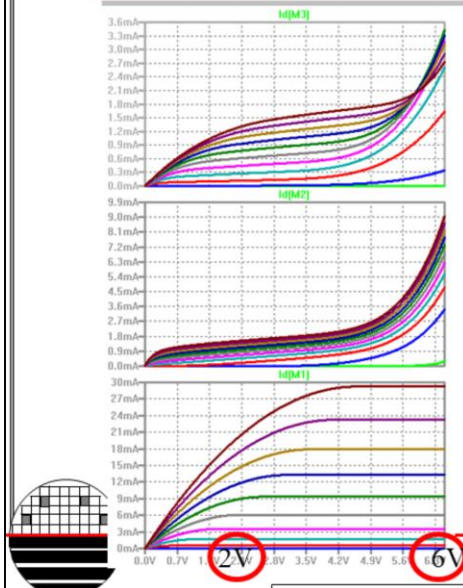


This shows simulated results for deep submicron transistors. We see that the EECMOSN model is the best model for L=0.25u transistors.



Again EECMOSN model best for deep submicron transistors.

## DEEP SUB-MICRON TRANSISTOR MODELS



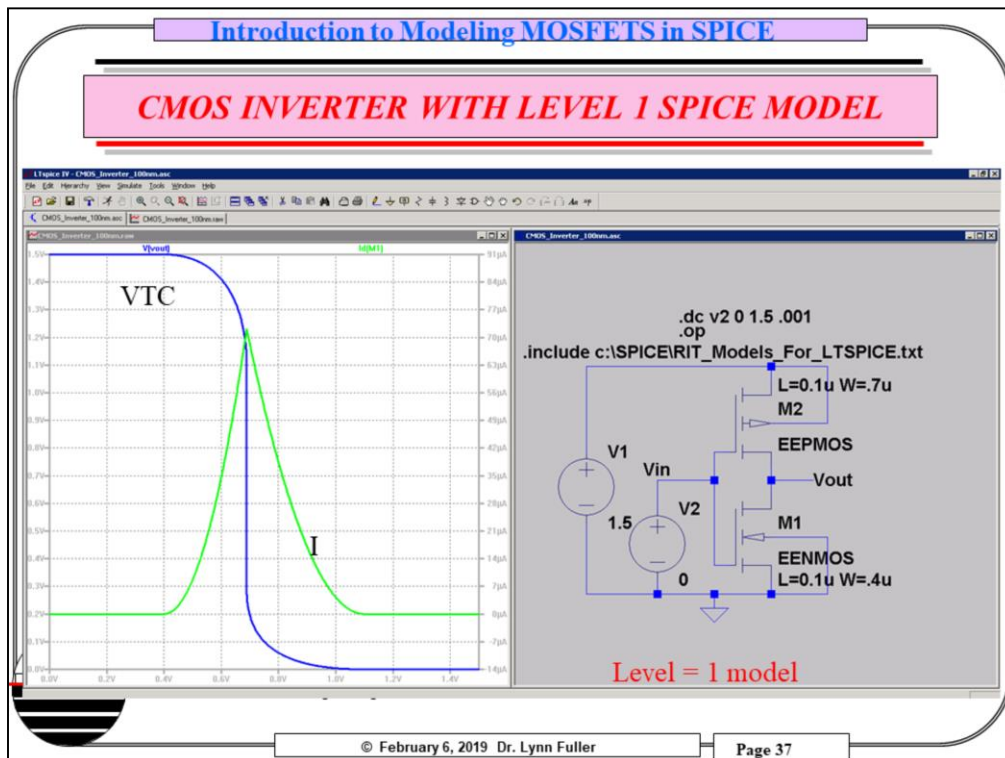
Deep sub-micron transistors show punch through at drain voltages over 3.3 volts. Which is correct.

Problem is worse in the sub-micron transistor because the channel is lighter doped.

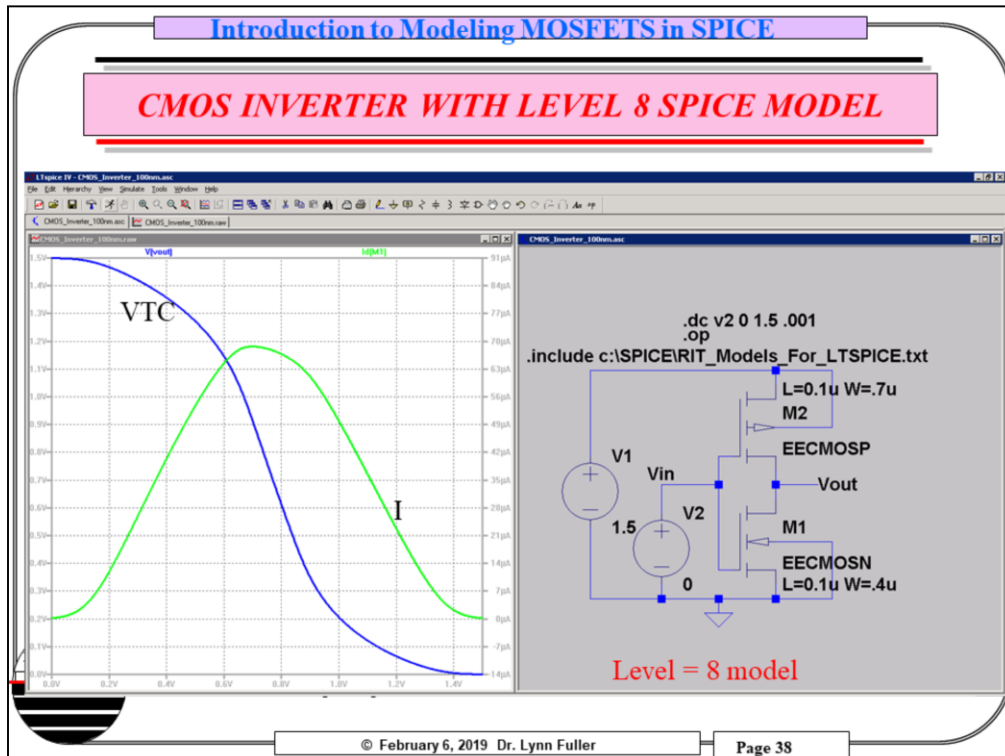
Simple model is incorrect.

Deep sub-micron transistors are normally operated at 3.3 volts or less.

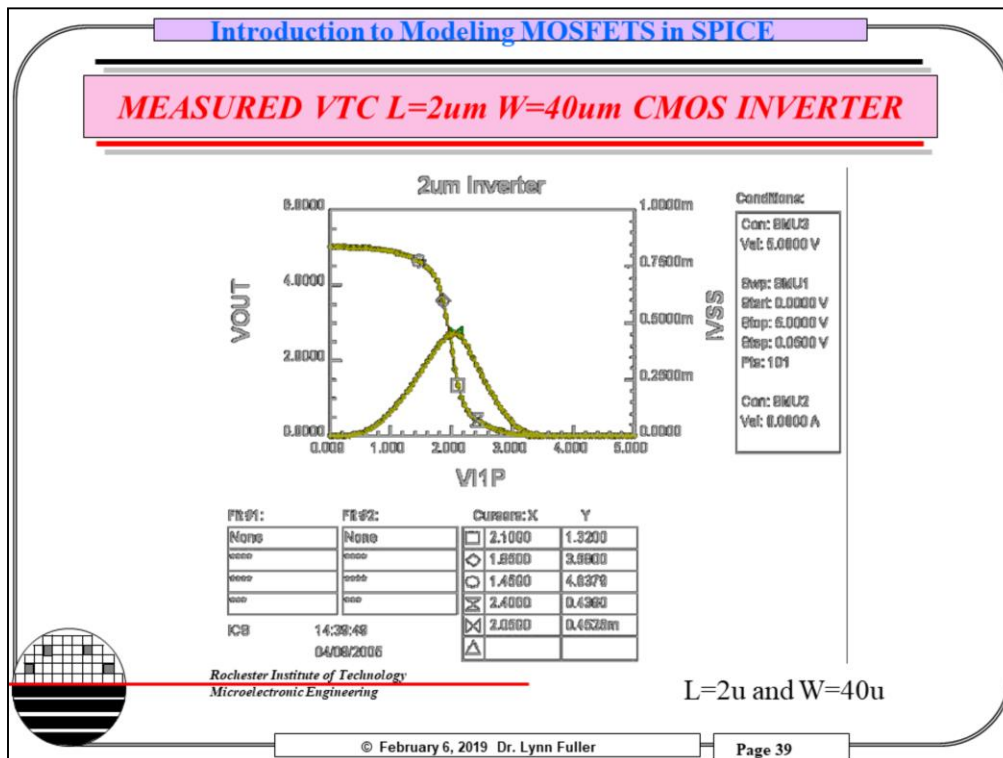




LEVEL=1 model Voltage Transfer Curve and Current.



LEVEL= 8 model Voltage Transfer Curve and Current.



Measured VTC and ID vs Vin for  $L=2\mu$  and  $W=40\mu$  CMOS Inverter

**CMOS  
Dual Complementary  
Pair Plus Inverter**  
High-Voltage Types (20-Volt Rating)

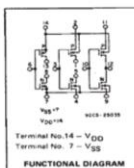
■ CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

**Features:**

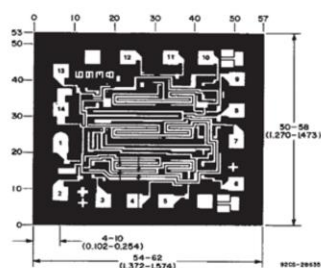
- Standardized symmetrical output characteristics
- Medium Speed Operation -  $t_{PHL}$ ,  $t_{PLH}$  = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Testative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C



**RECOMMENDED OPERATING CONDITIONS**

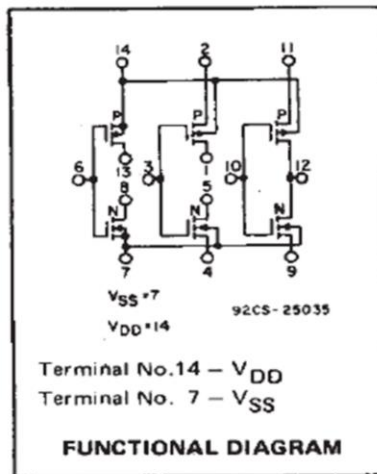
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ = Full Package Temperature Range)	3	18	V



**DIMENSIONS AND PAD LAYOUT FOR CD4007UBH**

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).



**FUNCTIONAL DIAGRAM**

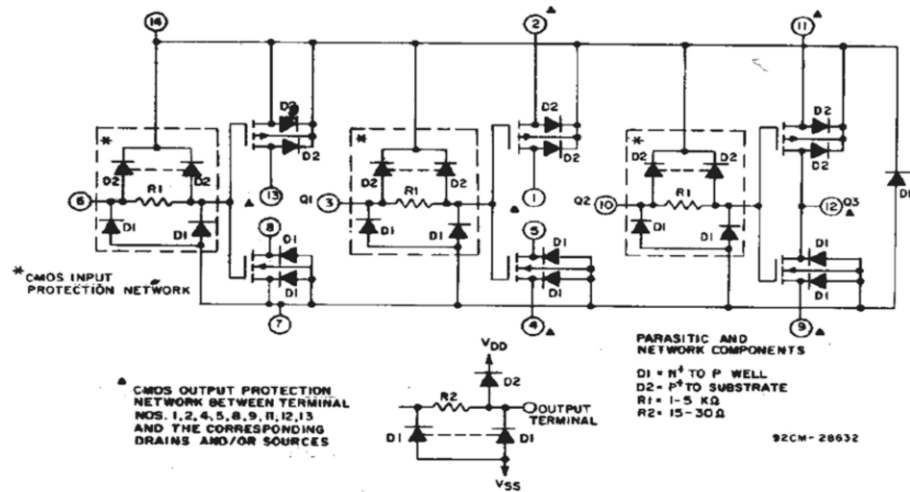
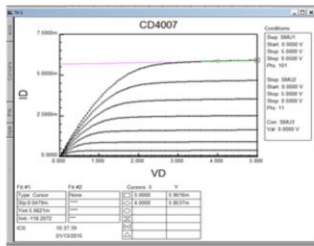


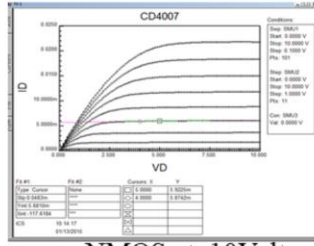
Fig. 1 — Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

This figure shows the parasitic diodes in the CD4007 chip. Each reverse biased diode represents a capacitance that should be included when doing SPICE transient analysis. The resistors along with the reverse biased diodes provide electrostatic discharge protection (ESD).

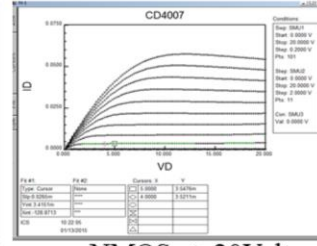
# Measured $I_D$ - $V_D$ s Family of Curves for 5, 10 and 20 volt Operation These measurement made using HP4145 Semiconductor Parameter Analyzer



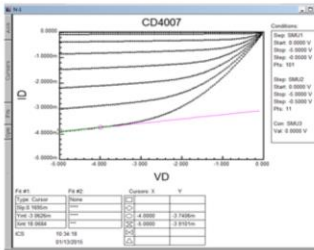
NMOS at 5Volts



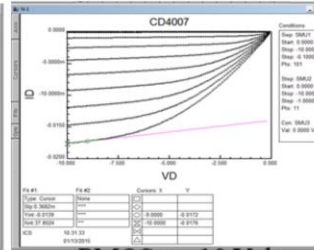
NMOS at 10Volts



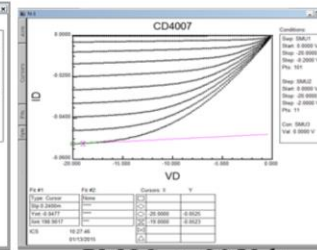
NMOS at 20Volts



PMOS at -5 Volts



PMOS at -10 Volts



PMOS at -20 Volts

```

*SPICE MODELS FOR RIT DEVICES AND LABS - DR. LYNN FULLER 8-17-2015
*LOCATION DR.FULLER'S COMPUTER
*and also at: http://people.rit.edu/lffeee
*
*-----
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=170u Ad=8500p As=8500p Pd=440u Ps=440u NRD=0.1 NRS=0.1
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=4E-8 XJ=2.9E-7 NCH=4E15 NSUB=5.33E15 XT=8.66E-8
+VTH0=1.4 U0= 1300 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=300 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-8 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=360u Ad=18000p As=18000p Pd=820u Ps=820u NRS=0.54
NRD=0.54
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-8 XJ=2.26E-7 NCH=1E15 NSUB=8E14 XT=8.66E-8
+VTH0=-1.65 U0= 400 WINT=1.0E-6 LINT=1E-6
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-8 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*-----

```

## ***SUMMARY***

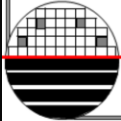
All of these examples are for DC characteristics but similar results would be shown for examples that depend on internal capacitors and resistors such as a study of rise-time, fall time, gate delay, oscillators, multi-vibrators, etc.

In general the third generation SPICE models for MOSFETS give better results.

Level=1 models are not good for MOSFETS with L less than 10um.

Large MOSFETS, SUB-MICRON MOSFETS and DEEP SUB MICRON MOSFET models have been introduced.

Models should be verified by comparing measured ID-VDS, ID-VGS, and Ring Oscillator output with SPICE simulated results.



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Please read.



**RING OSCILLATOR,  $t_d$ , THEORY**

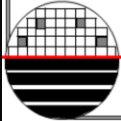
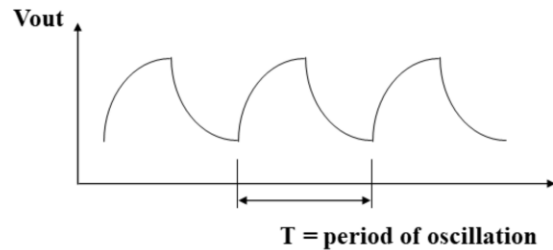
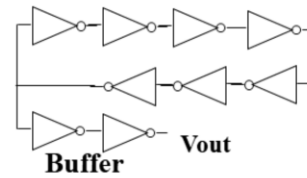
Seven stage ring oscillator  
with two output buffers

$$t_d = T / 2 N$$

$t_d$  = gate delay

$N$  = number of stages

$T$  = period of oscillation

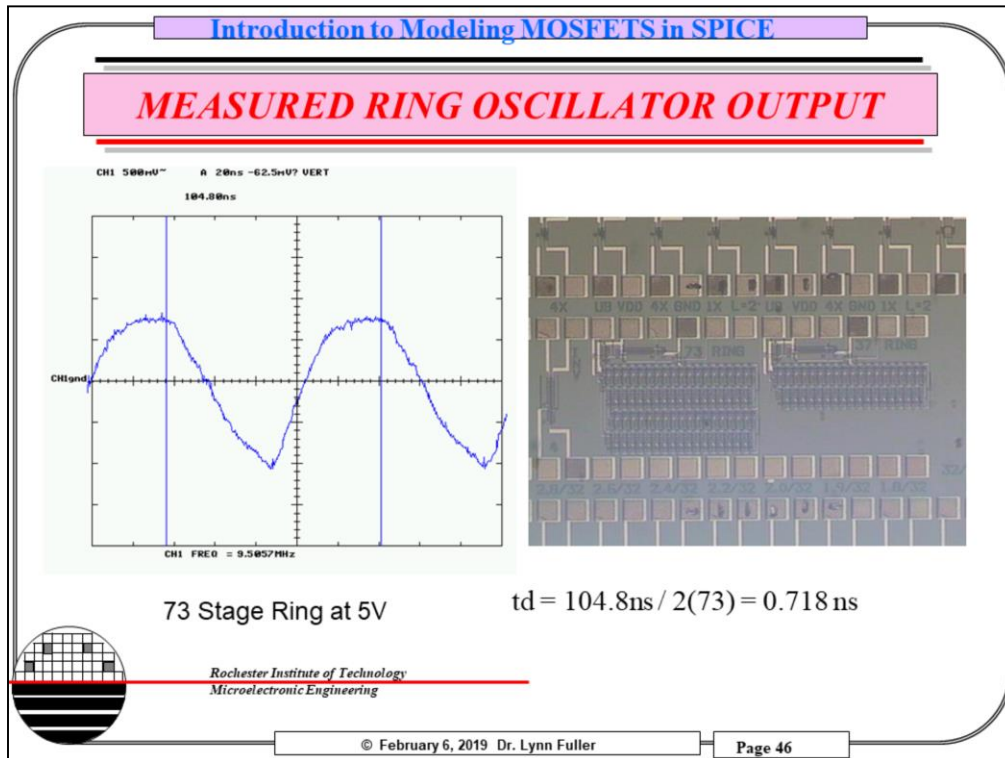


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A ring oscillator is an odd number of inverters in series with the output connected back to the input. It is used to measure the individual inverter gate delay by measuring the oscillator period and dividing by 2 times the number of stages in the ring oscillator. Today's fastest CMOS room temperature ring oscillators have gate delay of less than 10 ps.



Picture of a 73 stage ring oscillator and an oscilloscope capture of the output voltage.

**AC MODEL FOR MOSFETS**

The parameters that effect the AC response of a MOSFET are the resistance and capacitance values.

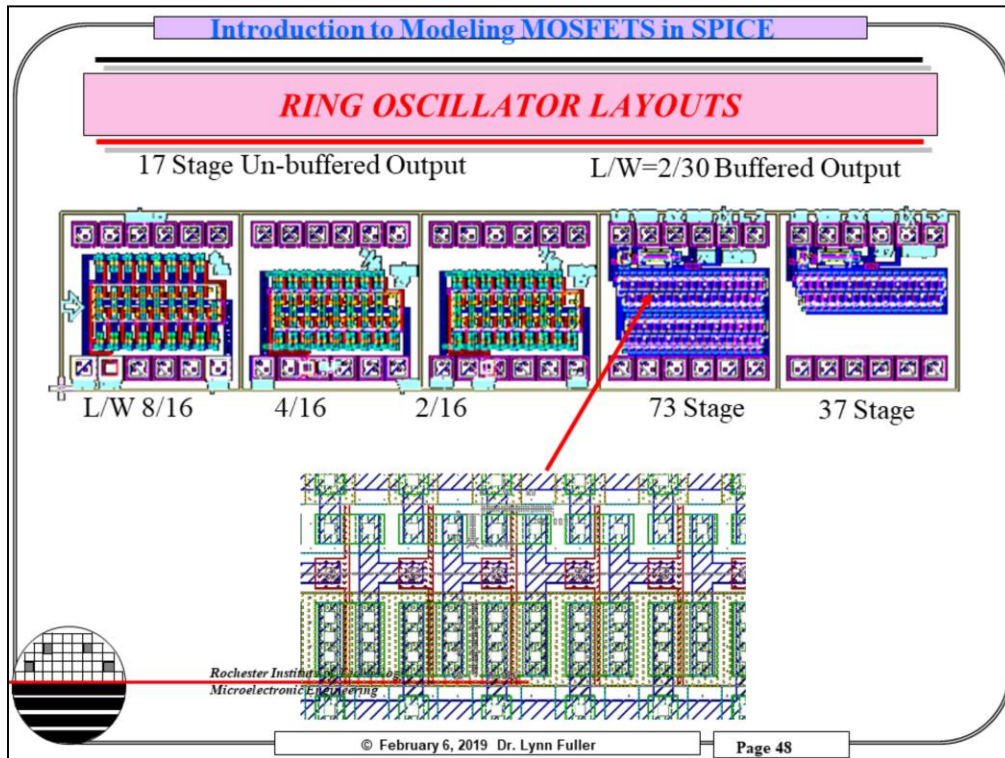
RS,RS	Source/Drain Series Resistance, ohms
RSH	Sheet Resistance of Drain/Source, ohms
CGSO,CGDO	Zero Bias Gate-Source/Drain Capacitance, F/m of width
CGBO	Zero Bias Gate-Substrate Capacitance, F/m of length
CJ	DS Bottom Junction Capacitance, F/m <sup>2</sup>
CJSW	DS Side Wall Junction Capacitance, F/m of perimeter
MJ	Junction Grading Coefficient, 0.5
MJSW	Side Wall Grading Coefficient, 0.5

These are combined with the transistors

L, W	Length and Width
AS,AD	Area of the Source/Drain
PS,PD	Perimeter of the Source/Drain
NRS,NRD	Number of squares Contact to Channel



To do a SPICE simulation these parameters need to be determined.



The 73 stage ring oscillator is one of the five different ring oscillators on the CMOS test chip.

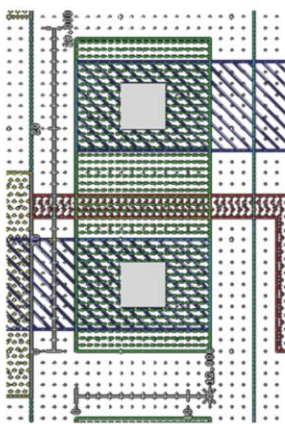
Introduction to Modeling MOSFETS in SPICE

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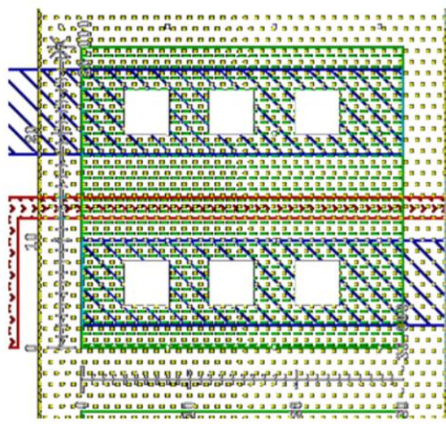
MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

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nmosfet



pmosfet



73 Stage Ring Oscillator



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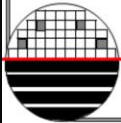
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Measurements of the NMOS and PMOS transistor layouts can be determined from these pictures.

***FIND DIMENSIONS OF THE TRANSISTORS***

	NMOS	PMOS
<b>L</b>	<b>2u</b>	<b>2u</b>
<b>W</b>	<b>12u</b>	<b>30u</b>
<b>AD</b>	<b>12u x 12u = 144p</b>	<b>12u x 30u = 360p</b>
<b>AS</b>	<b>12u x 12u = 144p</b>	<b>12u x 30u = 360p</b>
<b>PD</b>	<b>2x(12u + 12u) = 48u</b>	<b>2x(12u + 30u) = 84u</b>
<b>PS</b>	<b>2x(12u + 12u) = 48u</b>	<b>2x(12u + 30u) = 84u</b>
<b>NRS</b>	<b>1</b>	<b>0.3</b>
<b>NRD</b>	<b>1</b>	<b>0.3</b>

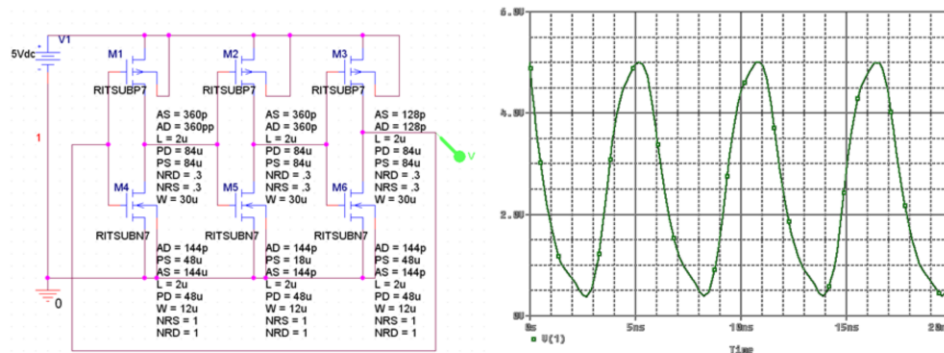
73 Stage



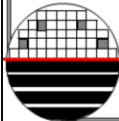
Use Ctrl Click on all NMOS on OrCad Schematic  
 Use Ctrl Click on all PMOS on OrCad Schematic  
 Then Enter Dimensions

These dimensions were obtained from measurements made on the layouts given on the previous page.

## SIMULATED OUTPUT AT 5 VOLTS



Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 5 volts



Measured  $t_d = 0.718 \text{ nsec @ } 5 \text{ V}$

$$t_d = T / 2N = 5.5 \text{ nsec} / 2 / 3$$

$$t_d = 0.92 \text{ nsec}$$

The transistor attributes were changed to reflect the dimensions found from the previous pages. The simulated oscillator output voltage is measured to get the period and the individual gate delay,  $t_d$ .

## CONCLUSION

Since the measured and the simulated gate delays,  $t_d$  are close to correct, then the SPICE model must be close to correct. The inverter gate delay depends on the values of the internal capacitors and resistances of the transistor.

Specifically:

$R_S$ ,  $R_D$ ,  $R_{SH}$

$CG_{SO}$ ,  $CG_{DO}$ ,  $CG_{BO}$

$C_J$ ,  $C_{JSW}$

These are combined with the transistors

$L$ ,  $W$  Length and Width

$AS$ ,  $AD$  Area of the Source/Drain

$PS$ ,  $PD$  Perimeter of the Source/Drain

$NRS$ ,  $NRD$  Number of squares Contact to Channel



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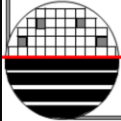
Page 52

## Conclusion



## REFERENCES

1. MOSFET Modeling with SPICE, Daniel Foty, 1997, Prentice Hall, ISBN-0-13-227935-5
2. Operation and Modeling of the MOS Transistor, 2nd Edition, Yannis Tsividis, 1999, McGraw-Hill, ISBN-0-07-065523-5
3. UTMOST III Modeling Manual-Vol.1. Ch. 5. From Silvaco International.
4. ATHENA USERS Manual. From Silvaco International.
5. ATLAS USERS Manual. From Silvaco International.
6. Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, with Mansun Chan, 3<sup>rd</sup> Edition, John Wiley, 2003, ISBN 0-471-59398-2
7. ICCAP Manual, Hewlet Packard
8. PSpice Users Guide.

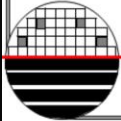
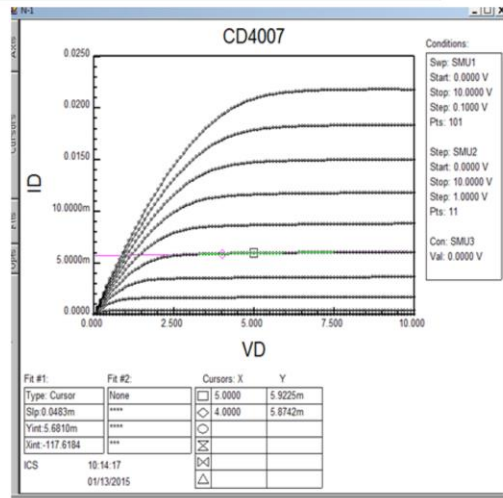


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## HOMEWORK – INTRO TO MOSFET SPICE MODELS

Use the CD4007 SPICE model on next page.

1. Use SPICE to generate the ID – VDS family of curves for 10 volts on the drain. Compare to the measured shown here.
2. Repeat for 20 volts
3. Use SPICE to generate a plot of ID versus VGS, show both ID and gm.



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This homework is due one week after this topic is presented in class.

## SPICE MODELS FOR CD4007 MOSFETS

*\*Used in Analog Electronics for CD4007 inverter chip*

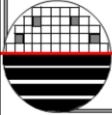
*\*Note: Properties L=5u W=170u Ad=8500p As=8500p Pd=440u Ps=440u NRD=0.1 NRS=0.1*

```
.MODEL RIT4007N7 NMOS (LEVEL=7  
+VERSION=3.1 CAPMOD=2 MOBMOD=1  
+TOX=6E-8 XJ=2.9E-7 NCH=4E15 NSUB=5.33E15 XT=8.66E-8  
+VTH0=1.4 U0= 925 WINT=2.0E-7 LINT=1E-7  
+NGATE=5E20 RSH=200 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-8 MJ=0.5 PB=0.95  
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5  
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)  
*
```

*\*Used in Analog Electronics for CD4007 inverter chip*

*\*Note: Properties L=5u W=360u Ad=18000p As=18000p Pd=820u Ps=820u NRS=0.54 NRD=0.54*

```
.MODEL RIT4007P7 PMOS (LEVEL=7  
+VERSION=3.1 CAPMOD=2 MOBMOD=1  
+TOX=6E-8 XJ=2.26E-7 NCH=3E15 NSUB=8E14 XT=8.66E-8  
+VTH0=-1.65 U0= 225 WINT=1.0E-6 LINT=1E-6  
+NGATE=5E20 RSH=800 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-8 MJ=0.5 PB=0.94  
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5  
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



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## SPICE MODELS FOR MOSFETS

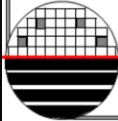
\* From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology

```
.MODEL RITSUBN7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
```

\*

\*From Sub-Micron CMOS Manufacturing Classes in MicroE ~ 1um Technology

```
.MODEL RITSUBP7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8
+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
```



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## SPICE MODELS FOR MOSFETS

\*4-4-2013 LTSPICE uses Level=8

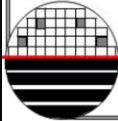
\* From **Electronics II EEEE482 FOR ~100nm Technology**

```
.model EECMOSN NMOS (LEVEL=8
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-9 XJ=1.84E-7 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=0.4 U0= 200 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
```

\*4-4-2013 LTSPICE uses Level=8

\* From **Electronics II EEEE482 FOR ~100nm Technology**

```
.model EECMOSP PMOS (LEVEL=8
+TOX=5E-9 XJ=0.05E-6 NCH=1E17 NSUB=5E16 XT=5E-8
+VTH0=-0.4 U0= 100 WINT=1E-8 LINT=1E-8
+NGATE=5E20 RSH=1000 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*
```



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