Testing – Device Problem Analysis

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2-7-2013 Testing-Device-Problem-Analysis.ppt
OUTLINE

Introduction
Good Device Characteristics
Various Not So Good Device Characteristics
Discussion of Characteristics
Design Errors
Fabrication Problems
INTRODUCTION

This document is a collection of test results showing problems with various semiconductor devices made in the microelectronics fabrication laboratory. The objective is to provide useful information for identification of the source of problems and to enhance the education of our students.
GOOD NMOS DEVICE CHARACTERISTICS

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**NMOS ID VS VGS**

- Conditions:
  - Con SMU1: Vol 8.000 V
  - Swp: SMU1
  - Start: 5.0000 V
  - Step: 5.0000 V
  - Step: 0.0500 V
  - Pts: 101
  - Con SMU2: Vol 0.0000 V
  - Con SMU3: Vol 0.0000 V

**NMOS SUB VT**

- Conditions:
  - Swp: SMU1
  - Start: 5.0000 V
  - Step: 5.0000 V
  - Step: 0.0000 V
  - Pts: 201

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**2/8=L/W Botom Right**

- Conditions:
  - Swp: SMU1
  - Start: 0.0000 V
  - Step: 0.0000 V
  - Step: 0.0000 V
  - Pts: 11
  - Con SMU3: Vol 0.0000 V
  - Con SMU4: Vol 0.0000 V
GOOD PMOS DEVICE CHARACTERISTICS

PMOSFET ID vs VGS

PMOSFET SUB VT

L/W = 2/4 PMOS

Conditions:
- Con. SMU1
  - Val. -0.1000 V
- Swap. SMU2
  - Start. -0.1000 V
  - Stop. -5.0000 V
  - Step. -0.4000 V
  - Pts. 101
- Con. SMU3
  - Val. 0.0000 V
- Con. SMU4
  - Val. 0.0000 V

Conditions:
- Con. SMU1
  - Val. -0.1000 V
- Swap. SMU2
  - Start. -0.1000 V
  - Stop. -5.0000 V
  - Step. -0.4000 V
  - Pts. 101
- Con. SMU3
  - Val. 0.0000 V
- Con. SMU4
  - Val. 0.0000 V
NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN SUB-CMOS PROCESS
Over etched contact cuts makes a non-ohmic (rectifying or Schottky) contact with the lighter doped n-type area of the drain/source. P-type devices have ohmic contacts.
CONTACTS TO SILICON

Ideal Ohmic
Al/p-silicon

Rectifying
Al/n-silicon

Tunneling Ohmic
Al/n+-silicon
NON OHMIC CONTACT TO NMOS DRAIN/SOURCE IN ADV-CMOS PROCESS

ID-VD for NMOS Transistor

\[ \text{L}_{\text{mask drawn}} = 0.6 \, \mu\text{m} \]
\[ \text{L}_{\text{effective}} = 0.4 \, \mu\text{m} \]

*This is RIT’s first sub-0.5 \, \mu\text{m} Transistor*

Mike Aquilino May 2004
Too much silicide formation makes a non-ohmic (rectifying or Schottky) contact with the lighter doped n-type area of the drain/source.
EFFECT OF SINTER ON IV CHARACTERISTICS

Before Sinter

After Sinter

Native Oxide
Different looking family of curves at different locations on the wafer

Family of curves for L=2µm MOSFETs

2µm/32µm L/W NMOS AND PMOS
NON UNIFORMITY IN PLASMA ETCH OF POLY

Family of curves for  
L=2µm MOSFETs

2µm/32µm L/W NMOS AND PMOS
Occasionally our 1um Devices Work
Why does the sub-threshold plot not flatten out at the bottom?

Answer: Vt is ~0.5 volt and swing is ~100mV/decade so at zero volts the device can be down 5 decades of current which is $10^{-10}$ it should flatten out at $\sim 10^{-11}$ or $10^{-12}$ …… need higher Vt or smaller swing
SHORT CHANNEL – BAD SUB THRESHOLD
DRAIN INDUCED BARRIER LOWERING

\[ \text{DIBL} = \frac{\text{change in } V_G}{\text{change in } V_D} \]

at \( ID = 1 \times 10^{-9} \text{ amps/µm} \) or \( 1.6 \times 10^{-8} \text{ amps} \) for this size transistor

\[ \approx \frac{(1.1957 - 1.1463)}{(5 - 0.1)} \]

\[ \approx 10 \text{mV/V} \]
MOBILITY DEGRADATION

Short channel

long channel
VELOCITY SATURATION

Short channel

long channel

Note: Id should increase with \((V_{gs}-V_{t})^2\) in long channel devices
Mark Klare 7/22/94 Electron beam direct write on wafer, n-well process 5E12 dose, P+ Poly Gate PMOS, shallow BF2 D/S implant, no Vt adjust implant.

L=0.75 µm  
Xox=300 Å  
D/S Xj = 0.25 µm  
P+ poly  
Nd well ~3E16  

Vt = -0.15  
Sub Vt Slope=130 mV/dec
WHAT IS WRONG?

NO CONNECTION
Switch Matrix Programmed Wrong
Switch Matrix Not Copied
Incomplete Contact Cut Etch
Aluminum Oxide Between M1 and M2
GOOD RESISTOR CHARACTERISTICS

Nwell Resistor

Poly Resistor

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IS THIS GOOD?

NO
Open Circuit, both electrical and visual evidence
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IS THIS GOOD?

NO

R \approx \frac{1}{m} = \frac{1}{0.03357} \approx 29,788 \text{ ohms}

which is 58 ohms/contact

512 Vias

m1-m2 Via Chain 512 Vias

NO

R = \frac{1}{m} \approx \frac{1}{0.03357} \approx 29,788 \text{ ohms}

which is 58 ohms/contact
**IS THIS GOOD?**

**512 Vias**

**YES**

M1-M2 Via chain with 512 Vias and total resistance of 118 ohms or 0.231 ohms per contact
WHAT IS WRONG?

Testing PMOS with NMOS-1 Setup

Testing PMOS with PMOS-1 Setup
WHAT IS WRONG?

Leff is almost zero
Poly over etched making L too small
PMOS works at L/W = 2/4 but not at 1/4
NON UNIFORMITY IN PLASMA ETCH OF POLY

Lot Number = F050118
Wafer Number = D3

Family of curves for
L=2µm MOSFETs

2µm/32µm L/W NMOS AND PMOS
SINGLE AND DUAL PHOTO CELL

Isc = 1.088 uA or 6 A/m²

Isc = 0.585 uA or 3.25 A/m²

Diode Characteristics Shifts Down with Light
Design Errors
N-Wells too close
N+ and P+ not correct
8-CELL PHOTO BATTERY

Design Errors Fixed Diode Characteristics Shifts Down with Light
WHAT IS WRONG WITH THIS DIGITAL CIRCUIT

Design Errors – Missing Contact Cuts
MASK DEFECTS
MASK DEFECT

This defect will cause a short through the pn junction of our solar cell.
LARGE 5mm X 5mm PHOTODIODE

Isc = 0.15mA (short circuit current)
or 9.09 A/m²
73 Stage Ring Oscillator

4X Buffer
L=2µm
5Volt Supply
Frequency = 4.37MHz
Period = T = 2N td = 230ns
td = 1.58ns

The Ring Oscillator Works
Is It Working Correctly?

Electrical Test Results
RING OSCILLATOR LAYOUTS

17 Stage Un-buffered Output  L/W=2/30 Buffered Output

L/W 8/16  4/16  2/16  73 Stage  37 Stage
MOSFETS IN THE INVERTER OF 73 RING OSCILLATOR

73 Stage Ring Oscillator

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### FIND DIMENSIONS OF THE TRANSISTORS

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>L</strong></td>
<td>2u</td>
<td>2u</td>
</tr>
<tr>
<td><strong>W</strong></td>
<td>12u</td>
<td>30u</td>
</tr>
<tr>
<td><strong>AD</strong></td>
<td>12u x 12u = 144p</td>
<td>12u x 30u = 360p</td>
</tr>
<tr>
<td><strong>AS</strong></td>
<td>12u x 12u = 144p</td>
<td>12u x 30u = 360p</td>
</tr>
<tr>
<td><strong>PD</strong></td>
<td>2x(12u+12u) = 48u</td>
<td>2x(12u+30u) = 84u</td>
</tr>
<tr>
<td><strong>PS</strong></td>
<td>2x(12u+12u) = 48u</td>
<td>2x(12u+30u) = 84u</td>
</tr>
<tr>
<td><strong>NRS</strong></td>
<td>1</td>
<td>0.3</td>
</tr>
<tr>
<td><strong>NRD</strong></td>
<td>1</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Use Ctrl Click on all NMOS on OrCad Schematic
Use Ctrl Click on all PMOS on OrCad Schematic
Then Enter Dimensions

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73 Stage
Three Stage Ring Oscillator with Transistor Parameters for 73 Stage Ring Oscillator and Supply of 5 volts

td = T / 2N = 5.5nsec / 2 / 3

Measured td = 1.580 nsec @ 5 V
REFERENCES

1. Dr Fuller’s webpage on CMOS testing, http://people.rit.edu/lffeee/CMOS.htm
2. other
HOMEWORK

1. Problem 1
2. other