VLSI Computer Aided Design (CAD)

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OUTLINE

The Design Process
Introduction
Schematic Level Design
Simulation
Technology Selection
Design Rules
Physical Design
References
Homework
STAGES IN THE DESIGN PROCESS

Problem Specification -> Behavioral Design or Truth Table
Logic Design -> Gate Level Schematic
Circuit Design -> Transistor Level Schematic
Simulation -> Output File

Technology Selection -> Design Rules, Layout Layers
Physical Design -> Layout

Maskmaking – Fabrication – Testing - Packaging
INTRODUCTION

This document is intended to lead the student through a simple digital circuit design with emphasis on the physical design (layout).
**EXCLUSIVE OR (XOR) DESIGN EXAMPLE**

Functional Description – This digital logic circuit returns a true (high) value when one of two inputs is high and returns a false (zero) otherwise.

<table>
<thead>
<tr>
<th>VA</th>
<th>VB</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Gate Level Design

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GATE LEVEL SIMULATION OF XOR – AND/OR

AND-OR Gate XOR

PULSE(0 1 0 5n 5n .5m 1m 2)

.tran 0 2m 0

PULSE(0 1 0 5n 5n 1m 2m 1)
**NOR CIRCUIT REALIZATION FOR XOR**

<table>
<thead>
<tr>
<th>VA</th>
<th>VB</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Exclusive OR (XOR) function:

- A XOR B = (A AND NOT B) OR (NOT A AND B)

Delta logic implementation:

```
A  B  |  A  |  B  |  NOT B  |  NOT A  |  A  AND NOT B  |  NOT A  AND B  |  OUT  
-----|-----|-----|---------|---------|---------------|--------------|------
0  0  | 0   | 0   | 1       | 1       | 0             | 0            | 0    
0  1  | 0   | 1   | 1       | 0       | 0             | 1            | 1    
1  0  | 1   | 0   | 0       | 1       | 1             | 0            | 1    
1  1  | 1   | 1   | 0       | 0       | 0             | 1            | 0    
```
GATE LEVEL SIMULATION OF XOR – ALL/NOR
TRANSISTOR LEVEL SIMULATION OF XOR – ALL/NOR
RIT Subµ CMOS

- 150 mm wafers
- $N_{\text{sub}} = 1 \times 10^{15} \text{ cm}^{-3}$
- $N_{\text{n-well}} = 3 \times 10^{16} \text{ cm}^{-3}$
- $X_j = 2.5 \mu m$
- $N_{\text{p-well}} = 1 \times 10^{16} \text{ cm}^{-3}$
- $X_j = 3.0 \mu m$
- LOCOS
- Field Ox = 6000 Å
- $X_{\text{oxygen}} = 150 \text{ Å}$
- $L_{\text{min}} = 1.0 \mu m$
- LDD/Side Wall Spacers
- 2 Layers Aluminum
- 3.3 Volt Technology
- VT’s = +/- 0.75 Volt
- Robust Process (always works)
- Fully Characterized (SPICE)
### MOSIS TSMC 0.35 2-POLY 4-METAL LAYERS

<table>
<thead>
<tr>
<th>MASK LAYER NAME</th>
<th>MENTOR NAME</th>
<th>GDS #</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>N WELL</td>
<td>N_well.i</td>
<td>42</td>
<td></td>
</tr>
<tr>
<td>ACTIVE</td>
<td>Active.i</td>
<td>43</td>
<td></td>
</tr>
<tr>
<td>POLY</td>
<td>Poly.i</td>
<td>46</td>
<td></td>
</tr>
<tr>
<td>N PLUS</td>
<td>N_plus_select.i</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>P PLUS</td>
<td>P_plus_select.i</td>
<td>44</td>
<td></td>
</tr>
<tr>
<td>CONTACT</td>
<td>Contact.i</td>
<td>25</td>
<td>Active_contact.i 48</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>poly_contact.i 47</td>
</tr>
<tr>
<td>METAL1</td>
<td>Metal1.i</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>VIA</td>
<td>Via.i</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>METAL2</td>
<td>Metal2.i</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>VIA2</td>
<td>Via2.i</td>
<td>61</td>
<td>Under Bump Metal</td>
</tr>
<tr>
<td>METAL3</td>
<td>Metal3.i</td>
<td>62</td>
<td>Solder Bump</td>
</tr>
</tbody>
</table>

These are the main design layers up through metal two.
## MORE LAYERS USED IN MASK MAKING

<table>
<thead>
<tr>
<th>LAYER</th>
<th>NAME</th>
<th>GDS</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>cell_outline.i</td>
<td>70</td>
<td>Not used</td>
</tr>
<tr>
<td></td>
<td>alignment</td>
<td>81</td>
<td>Placed on first level mask</td>
</tr>
<tr>
<td></td>
<td>nw_res</td>
<td>82</td>
<td>Placed on nwell level mask</td>
</tr>
<tr>
<td></td>
<td>active_lettering</td>
<td>83</td>
<td>Placed on active mask</td>
</tr>
<tr>
<td></td>
<td>channel_stop</td>
<td>84</td>
<td>Overlay/Resolution for Stop Mask</td>
</tr>
<tr>
<td></td>
<td>pmos_vt</td>
<td>85</td>
<td>Overlay/Resolution for Vt Mask</td>
</tr>
<tr>
<td></td>
<td>LDD</td>
<td>86</td>
<td>Overlay/Resolution for LDD Masks</td>
</tr>
<tr>
<td></td>
<td>p plus</td>
<td>87</td>
<td>Overlay/Resolution for P+ Mask</td>
</tr>
<tr>
<td></td>
<td>n plus</td>
<td>88</td>
<td>Overlay/Resolution for N+ Mask</td>
</tr>
<tr>
<td></td>
<td>tile_exclusion</td>
<td>89</td>
<td>Areas for no STI tiling</td>
</tr>
</tbody>
</table>

These are the additional layers used in layout and mask making.
**MOSIS LAMBDA BASED DESIGN RULES**

http://www.mosis.com/design/rules/

If \( \lambda = 1 \, \mu m \) then contact is \( 2 \, \mu m \times 2 \, \mu m \)
MOSIS LAMBDA BASED DESIGN RULES

http://www.mosis.com/design/rules/

MOSIS Educational Program

Instructional Processes Include:
AMI $\lambda = 0.8 \, \mu m$ SCMOS Rules
AMI $\lambda = 0.35 \, \mu m$ SCMOS Rules

Research Processes:
go down to poly length of 65nm
Using the VLSI Lab Workstations and Mentor Graphics CAD Tools

Usually the workstation screen will be blank, press any key to view a login window. Login or switch user and then login.

Login: username (RIT computer account)
Password: ********

The screen background will change and your desktop will appear. On the top of the screen click on Applications then System Tools then Terminal. A window will appear that has a Unix prompt inside.

Type `source /tools/env.d/mentor.sh` ENTER
response is grumpy cat is grumpy

Type `ic <RET>`, it will take a few seconds, then the Pyxis Layout user interface will appear. Maximize the Pyxis Layout window.
We have set up a shared folder for this course that has primitive cells which you can open, add or copy for your designs.

/tools/ritpub/mcee550/

Students and faculty for this course have their own personal accounts where they can keep their designs.

/home/username/filename/

All users have access to some public folders that have files for processes, design rules, etc.

/tools/ritpub/process/fuller
It is convenient to show the Layer Palette and Session banners on the right side of the workspace. If they are not visible go to Setup > Windows> and check Layer Palette and Session. You should also check Command Shell, Message Area and Status Line.
In the session menu palette on the right hand side of the screen, under Layout, select New, using the left mouse button. (also under file on top banner) For cell name type name-device. Set the process by typing (or browse) /tools/ritpub/process/fuller in the process field. Leave the Rules field blank. Click OK

At the top left of the window check that the process is fuller not Default. If not correct go to top banner click on Context>Process>Set Process

The Layer Palette should now show the layers you expect to used for your device layout.

On top banner select Setup>Preferences>Display>Rulers/Grid
Set Snap to 1 and 1 as shown. (or other values as necessary)
The plus mark + is (0,0) the small dots are the 1 um grid the large dots are the 10um grid. The mouse curser is shown by the diamond and is at (-3um,+3um) as indicated by the cursor position at the top of the workspace.
ADDING PAD CELL AND LETTERS

To add a cell to a design select Add > Instance and type Q
The window shown should pop up
You can browse to the cell you want to add then
Select OK

Shortcut keystrokes
M = move
C = copy
D = delete
Q = add cell or edit object
U = undo
COPYING CELL FROM SHARED FOLDER

Your Cell Design

Selected Shared Folder Cell
PASTING PRIMITIVE CELLS INTO YOUR CELL DESIGN
**LAYOUT – GATE ARRAY**

Green is Active
Dashed Yellow is N-Well
Red is Poly
Blue is Metal-One
Pink is Metal-Two
White is Contact Cut
Yellow is Via
P and N select not shown
1. Cells are separated from adjacent cells by off transistors
2. Well contacts are made at each of the off transistors
3. Metal-two connects thru Via to Metal-one
4. Metal-one connects thru Contact Cuts to active and Poly
5. Inputs and Outputs connections are made vertically with Metal-two
6. Routing channels exist above and below the gate array and contain horizontal metal-one interconnects between cells, with Via to Metal-two.
7. The NULL cell at the end of the gate array row satisfy design rules for extension of well beyond active, etc. It also provides a vertical routing channel which may be useful in constructing macro cells.
INTERCONNECTING PRIMITIVE CELLS

The primitive cells are interconnected using Metal-1 and Metal-2 in the routing channels above and below the primitive cells. First place horizontal metal lines in the routing channels by creating a shape with the following command (type anywhere in the drawing window)

```
$add_shape([[0,166],[368,172]],49)
```

This will draw a box with lower left corner at x=0, y=166 and upper right corner at x=368um, y=172um, with layer number 49 (metal-1). This should be a horizontal metal-1 interconnect line at the top of your cell if you placed the lower left corner of your cell at (0,0)

Both M1 and M2 will need some type of contact cut or Via. See next page for examples
M1 AND M2 INTERCONNECTS

At this level of zoom you can not see the Vias between M1 and M2.
CONNECTIONS BETWEEN M1 AND M2

6um wide metal lines for M1 and M2 with 2umx2um Vias
CONNECTIONS TO ACTIVE AND POLY

Metal-2 to Via to Metal-1 to CC to Active

Metal-2 to Via to Metal-1 to CC to Poly
USING THE HP WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS – SELECTING OBJECTS

Select easy edit, Select Shape. Draw boxes by click and drag of mouse. Unselect by pressing F2 function key. The highlighted layer in the layer palette is selected prior to drawing. Unselect by pressing F2. Exit drawing by pressing ESC.

Selecting multiple objects is defined in Setup>Selection

Unclick Surrounding the select rectangle to not select the cell outline.
DRAWING BOXES AND OTHER SHAPES

Select easy edit, right click and select Show Scroll Bars, scroll through the various edit commands.

DRAW BOXES by click and drag of mouse. Unselect by pressing F2 function key. The following command will draw a 3000 µm by 3000 µm box with layer 4 color/shading. Put the cursor in the workspace and start typing. A text line window will pop up. If the command has a typo just start typing again and use the up arrow to recall previous text.

$add_shape([[0,0],[3000,3000]],4)

The Notch command is useful to change the size of a selected box or alter rectangular shapes into more complex shapes.
DRAW CIRCLES by typing `$set_location_mode(@arc)` return. The following command will draw a 100µm radius circle centered at (0,0) using 300 straight line segments.

$add_shape($get_circle([0,0],[100,0],300),3)

To reset to rectangles type `$set_location_mode(@line)` return.

MOVE, COPY, DELETE, NOTCH, etc: Selected objects will appear to have a bright outline. Selected objects can be moved (Move), copied (Copy), deleted (Del), notched (Notc). When done unselect objects, press F2.

Change an Object to another layer: Selected object(s) click on Edit on the top banner, select Change Attributes, change layer name to the name you want. When done press F2 to unselect
USING THE HP WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS - OTHER

ZOOM IN OUT: pressing the + or - sign on right key pad will zoom in or out. Also pressing \texttt{shift + F8} will zoom so that all objects are in the view area. Select \texttt{View} then \texttt{Area} and click and drag a rectangle will zoom so that the objects in the rectangle are in the view area.

MOVING VIEW CENTER: pressing the middle mouse button will center the view around the pointer.

ADDING TEXT: Add > Polygon Text click on layout where you want it located. Select the text box and Edit > Change > Attributes, change pgtext, change scale to 3.0

SCREEN PRINT: Click on MGC and select \texttt{Capture Screen}. Enter file name and location such as \texttt{Lynn.png} and \texttt{Desktop}. After saving you can use a flash drive and transfer the file to another computer.

LOG OUT: upper right of screen click on name and select LOG OUT
## BASIC UNIX COMMANDS

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ls</td>
<td>list the files and directories in the current directory</td>
</tr>
<tr>
<td>cd</td>
<td>change directory</td>
</tr>
<tr>
<td>cd ..</td>
<td>go up one directory</td>
</tr>
<tr>
<td>mv</td>
<td>move a file (rename a file)</td>
</tr>
<tr>
<td>rm</td>
<td>remove a file (delete a file)</td>
</tr>
<tr>
<td>pwd</td>
<td>display path of current directory</td>
</tr>
<tr>
<td>mkdir</td>
<td>create a new directory</td>
</tr>
<tr>
<td>rmdir</td>
<td>remove a directory</td>
</tr>
<tr>
<td>yppasswd</td>
<td>change your password</td>
</tr>
</tbody>
</table>

It is important to remember that since this is a UNIX operating system, the commands are case sensitive.
GDS FILE GENERATION

Once the cell design is completed export the GDS file for maskmaking. Select **Translate** on the top banner and then **Write GDSII**. Output file needs full path name and `.gds` extension.

Cell layout name

Save to your desktop
EXPORT CELL DESIGN AS GDS II FILE

Export as filename.gds
Email to Dr. Fuller
lffeee@rit.edu

Cell layout name

Save to your desktop
## MASK ORDER FORM

### Details
- **Design File Name (.gds)**: mems-2014-final.gds
- **Membrane Size**: 16.5mm x 16.5mm

### Mask Type Needed
- **Contact Aligner**
  - Max field size: 105mm x 105mm
  - Mask Size: 5” x 5” x 0.09” Soda Lime
  - Orientation: Mirror 90
  - Fracture Resolution: 0.5μm
- **GCA Stepper**
  - Max field size: 20mm x 20mm
  - Mask Size: 5” x 5” x 0.09” Soda Lime
  - Orientation: Mirror 135
  - Fracture Resolution: 0.5μm
- **ASML Stepper**
  - Max field size: 22mm x 22mm
  - Mask Size: 6” x 6” x 0.12” Quartz
  - Orientation: Mirror 90
  - Fracture Resolution: 0.5μm

### Additional Information
- **Multiple Field Array Plate**
- **Notes**: If multiple design files are to be incorporated into your array, please specify the array layout separately. Your designs will be butted together from the array unless otherwise specified.

---

Dr Fuller
RIT
INVERTER

Vin ——— Vout

+V

Idd

PMOS

Vin ——— Vout

NMOS

CMOS

<table>
<thead>
<tr>
<th>VIN</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

W = 40 µm
Ldrawn = 2.5µm
Lpoly = 1.0µm
Leff = 0.35 µm
PRIMITIVE CELLS
MEBES - Manufacturing Electron Beam Exposure System

Maskmaking Tool
FILE FORMATS

Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only
REFERENCES

This assignment can be done using the tools in the VLSI lab. Ideally the switch level simulation and SPICE simulations are also done with the tools in the VLSI Lab.

Design a 4 to 1 multiplexer. Two inputs (Input A and Input B) select which one of four other digital inputs (I1 I2 I3 I4) is output (Vout)

Document the following items, Truth Table, Gate Level Schematic, Gate Level Simulation, Transistor Level Schematic, Transistor Level Simulation, Layout using Gate Array, Including connections to 12-pad Pad Frame.
4 TO 1 MULTIPLEXER

\[ \begin{align*}
I_0 & \quad A \\
I_1 & \quad \text{AUX} \\
I_2 & \quad \text{AUX} \\
I_3 & \quad \text{AUX} \\
\end{align*} \]

Q
4 TO 1 MUX - GATE LEVEL SIMULATION
4 TO 1 MUX – LAYOUT
4 TO 1 MUX – PEEKED AND ZOOM