Isolation Technology

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ISOLATION TECHNOLOGIES FOR BIPOLAR INTEGRATED CIRCUITS
STANDARD BURIED COLLECTOR
TRIPLE DIFFUSED PROCESS
COLLECTOR DIFFUSED
MESA

ISOLATION TECHNOLOGIES FOR MOS INTEGRATED CIRCUITS
GROW OXIDE AND ETCH
SEMI RECESSED LOCOS
FULLY RECESSED LOCOS
BIRDS BEAK ENCROCHMENT
PROBLEMS
ETCHED BACK LOCOS
POLY BUFFERED LOCOS
SILO
POP-SILO
SWAMI

SPOT
FUROX
BURIED-OXIDE ISOLATION
SHALLOW TRENCH
DEEP TRENCH
FIELD SHIELD
SILICON ON INSULATOR
WAFER BONDING
SILICON ON SAPPHIRE
SIMOX
MESA
The main idea is to build transistors on the same substrate, that are electrically isolated from each other. To do this the transistors are usually surrounded by a reverse biased pn junction or surrounded by an insulator or in the case of MOS devices “ringed” by a thick oxide layer.
JUNCTION ISOLATION IN STANDARD BURIED COLLECTOR PROCESS

N-type active area is surrounded on four sides and bottom by a reverse biased pn junction - isolating one active area from another.

Lateral Diffusion equals Epi Thickness
Disadvantage is size (area used) for Isolation.
COLLECTOR DIFFUSED ISOLATION

Improved Packing Density
Lower Breakdown Voltage (space charge layer is on the lighter doped side - the base side)
Higher parasitic junction capacitance
TRIPLE DIFFUSED ISOLATION

P-Type silicon
Thick Oxide and Channel Stop (in p-well) keeps parasitic transistor off. For n-well CMOS channel stop is in p-substrate.
Local Oxidation of Oxide (LOCOS) gives a step height about 1/2 of the “grow oxide and etch isolation” approach.
SEMIRECESSED LOCOS

This is what we use at RIT in the p-well CMOS process

Pad Oxide

Nitride

Pad oxide should be at least 1/3 nitride thickness to work as a stress relief layer

Etch nitride and pad oxide, implant channel stop if needed

Grow field oxide
Lateral oxide growth can be 0.5 µm to 0.1 µm, formation of “bird’s beak”
SEMIRECESSED LOCOS DETAILS

Pad oxide should be at least 1/3 nitride thickness to work as a stress relief layer.

Nitride thickness needs to be thick enough to not be consumed during field oxide growth.

Etching off nitride and pad oxide after field oxide is often done wet. Top of nitride is oxidized so it needs an HF etch followed by Hot (200 C) Phosphoric Acid etch or plasma etch.

Kooi oxide growth is a sacrificial oxide to clean up any silicon nitride formed under the pad oxide by diffusion of NH$_3$ (from water nitride reaction) through pad oxide.
KOOI (SACRIFICIAL) OXIDE

White ribbon problem

2 μm
LOCOS
SiO₂

1000 Å gate oxide

Si

1 μm
Bird’s beak encroachment limits the scaling of channel widths to ~1.5 µm
LOCOS BIRDS’ BEAK

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Note: at y = 0.2 µm in from the edge the oxidation rate is ~0.1 µm/hr for 500 Å pad oxide, so for a 2 hr oxide growth the pad oxide will grow ~ 0.2 µm compared to a 100 Å pad oxide with growth rate of almost zero.
LOCOS PROBLEMS

Boron channel stop implant encroachment in addition to oxide encroachment into the active region

Stress induced damage
The yield strength of silicon is 7E9 Pascals
The stress can be large enough to cause damage in the silicon at the edge of the LOCOS. The D/S junctions are also located at the edge of the LOCOS. The result is that the junctions are leaky.

Stress increases with increased nitride thickness, increased field oxide thickness and decreased pad oxide thickness. In the RIT Pwell CMOS process pad oxide is 500 Å, nitride is 1500 Å and field oxide is 11,000 Å. We may get more reliable results by decreasing the nitride to 1000 Å and decreasing the field oxide to 8000 Å.
The etch back reduces topology and birds beak but eventually exposes the channel stop implant in the p-type substrate or well field areas. (important for width)
FULLY RECESSED OXIDE LOCOS

- Nitride
- Pad Oxide
- Etch Silicon
- Birds Head

Field Oxide
FULLY RECESSED LOCOS – BIRD’S HEAD
POLY BUFFERED LOCOS

Poly layer reduces stress and produces birds beak of only 0.1 to 0.2 µm
POLY BUFFERED LOCOS

Crab Eyes
Sealed Interface Local Oxidation - SILO
Thin Nitride directly on Silicon, then Low Temp Oxide, then 2nd Nitride, then etch the silicon a little before FOX

Need to etch silicon to reduce the surface topology. This process gives a steeper step than normal LOCOS
PROTECTIVE OXIDE PAD - SILO (POP-SILO)

- 2nd Nitride layer
- Low Temperature Oxide ~1500 Å
- 1st Nitride Layer ~800 Å
- Pad oxide ~125 Å

Second nitride layer thickness chosen to give spacer of 0.25 µm

Field Oxide
SWAMI - Hewlett-Packard

Stress relief pad oxide, 1st nitride layer
silicon etch and field implant

2nd Nitride and LTO

RIE etch of LTO

Nitride Etch

Final Result

Grow Field Oxide
**Isolation Technology**

**SPOT**

1st FOX

Etch 1st FOX

Grow 2nd Pad Ox

LPCVD 2nd nitride

RIE nitride and oxide

Grow final FOX
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FUROX

LTO 1000 Å
Nitride 800 Å
Pad Oxide 200 Å

FOX 4500 Å

Nitride 400 Å
Oxide 100 Å

FOX 7700 Å

RIE
NON-LOCOS ISOLATION

Trench Etch and Refill
- Replace LOCOS
- Replace Deep Diffusion Isolation
- Used to prevent latchup in CMOS
- Used to combine Isolation and Capacitor formation in DRAM structures

Shallow Trench and Refill (0.5-0.8 µm)
- BOX

Moderate Depth Trench (~2 µm)
- U Groove

Deep Trench (>3 µm)
**BOX (BURIED-OXIDE) ISOLATION**

1. **1st Photoresist, flowed**
2. **Etch Shallow Trench**
3. **LTO Deposition**
4. **Planarizing RIE etches resist and LTO at same rate**

- Oxide
- 4000 Å
- 2nd Photoresist layer
MODIFICATIONS TO IMPROVE BOX

Improvements:

Void formation can occur if trenches are narrower than 2 um. High Temperature LPCVD of SiO2 helps.

Inversion of silicon sidewalls of p type active areas is possible so angled Boron Ion Implant or Spin on Dopant source is used to dope side walls with Boron.

Uniformity is hard to control. Since it is non uniform the SiO2 must be over etched leaving downward step in active area causing other problems.
BURIED OXIDE WITH ETCH STOP BOXES

Mo 2500 Å
Nitride 250 Å
Pad Oxide 150 Å

Thin Thermal Oxide and LTO Deposition
RIE Etch, Stop on Mo
Remove Mo, Nitride and Pad Ox
Etch Shallow Trench

This process avoids exposed downward step at edge of the active areas
U-grove if made with anisotropic wet etch (KOH/Isopropyl-alcohol) followed by dry anisotropic etch. The trench is filled with thermally grown oxide 0.4 um, nitride and polysilicon.

Toshiba is all dry etch and refill thermal oxide and poly.

note: poly refill can not be used for trenches of different width
DEEP TRENCH ISOLATION

Deep trench

2.5 μm

oxide

poly

n- epi

p+  p-sub

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FIELD SHIELD ISOLATION

Useful in high voltage devices because the substrate dopings are not increased to make a channel stop. (Increased doping reduces breakdown voltage) Instead a poly layer over the field region is connected to a negative voltage to keep the surface from inverting.
Dielectric Isolation
Wafer Bonding SOI
Silicon on Saphire
SIMOX
DIELECTRIC ISOLATION

1. n-type Silicon
2. Open Windows
3. Grow Oxide
4. Etch Silicon and Strip Oxide
5. Grow Oxide
6. Flip and Polish down to Insulator
7. Deposit Thick Poly Layer
8. Build Devices
WAFER BONDING SOI

Starting Wafer
Form V-grooves
Deposit Poly

Planarize

Grow Oxide

Flip and Bond Wafer
Thin and Polish
Build Devices

Starting Wafer

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WAFFER BONDING

Two oxidized-silicon wafers pressed together and subjected to an oxidizing ambient of 700 C (requires applied pressure)

With an applied Voltage and temperatures of 1100 to 1200 C

One oxidized wafer and one bare wafer are cleaned in H2O2 + H2SO4, rinsed and dried, After drying the wafers are placed face-to-face at room temperature. A self-adhesive contact is formed. Bonding is completed by a 4 hour 1100 C heat treatment in nitrogen.
**SOS - SILICON ON SAPPHIRE**

Thin layer of single crystal silicon, combined with trench isolation, to make isolated devices.

Starting Sapphire wafer, $\text{Al}_2\text{O}_3$, Single crystal and a Silicon epitaxial layer can be grown on it.
SIMOX - SEPARATION BY ION IMPLANTED OXYGEN

Implanted Oxygen or Nitrogen Ions

Thin layer of single crystal silicon, combined with trench isolation, to make isolated devices

1 Million Electron Volt, High Dose (2E18) Implant, to Make a Buried Dielectric Layer of SiO$_2$ or Si$_3$N$_4$, Also 200KeV, High Dose Implant followed by anneal and Epi Growth
REFERENCES

3. The Invention of LOCOS, Else Kooi, Institute of Electrical and Electronic Engineers, Inc., NY, NY 1991
HOMEWORK - ISOLATION

1. Discuss the problems with isolation by the standard LOCOS process.
2. In reference to the RIT p-well CMOS process sketch the cross section of the active area of a 1.0 micrometer transistor showing bird’s beak encroachment. Scale the sketch using the appropriate figures from the lecture.
3. What is the advantage of poly buffered LOCOS?
4. What is the difference between Sealed-Interface-Local-Oxidation (SILO) and Protective-Oxide-Pad SILO?
5. What is the advantage of the SWAM, SPOT and FUROX processes?
6. Describe trench isolation. What is the main advantage of trench isolation over local oxidation approaches?
7. Describe four approaches to silicon on insulator isolation technologies.