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OUTLINE

Introduction
  Fabrication vs Manufacturing
  Manufacturing Early 1990’s, Today, Tomorrow
Semiconductor Manufacturing Includes:
  Factory Modeling: Logistics (Scheduling), Ramp Up
  Factory Floor Control, WIP Tracking
  Cycle Time Management
  Contamination Free Manufacturing, Yield, Metrology, Test
  Process Integration, Evolution and Improvement,
    Advanced Processes, Technology Transfer
  TQM, CIM, SPC, 6 Sigma Manufacturing, DOE,
    Statistical Thinking
  Cost Containment

Human Resources
  Undergraduate Education
  University IC Labs
FABRICATION involves the design and realization of a semiconductor device or circuit. The goal is achieved if one device or circuit is made to work. Research is centered on new technologies and materials, new, smaller and faster devices, novel circuits, etc.

MANUFACTURING involves the realization of a large number of semiconductor devices or circuits. The goal is achieved if large numbers of circuits are made, at low cost (at a profit), with high yield and quick turn around time. Research is centered on manufacturing methodology, operations research, statistical process control, factory simulation, process integration, etc.
SEMICONDUCTOR MANUFACTURING IN 1991

NUMBERS FROM A MEDIUM SIZE SEMICONDUCTOR PLANT AT INTEL WITH 5000 WAFER STARTS/WEEK, 0.7 µm PROCESS

5000 WAFERS 150 mm DIAMETER PER WEEK
7 DAYS/WEEK, 24 HOURS/DAY OPERATION
300 EMPLOYEES
COST OF PLANT $500 MILLION
LIFE OF PLANT 5 YEARS
WAFER LOT SIZE = 25
COST OF PROCESSING ONE LOT = $25,000
SALES VALUE OF ONE LOT = $100,000  ($2.8 MILLION/DAY)
TIME IN MANUFACTURING = 40 DAYS
DISTANCE TRAVELLED IN FAB = 6 MILES
13 PEOPLE TO JUST MOVE, LOAD, UNLOAD MACHINES
MACHINE LOAD AND UNLOAD CYCLES = 6.8 MILLION/YEAR
20,000 MACHINE LOAD AND UNLOAD PER DAY
WORK IN PROCESS = 15,000 WAFERS
VALUE OF WORK IN PROCESS = $60 MILLION

SOURCE: E. SHAMAH MAY 1991, SRC PRESENTATION
PARTIAL CIM
TUNNEL AND CHASE FACILITY DESIGN
CASSETTE TO CASSETTE
LIMITED AUTOMATIC MATERIALS MOVERS
OUTPUT PARAMETER SPC
EXSITEU METROLOGY
BATCH PROCESSING
CLASS 10 TO 1 VLF
LIMITED INTEGRATED PROCESS TOOLS
90% FAB YIELD
60% SORT YIELD
40% EQUIPMENT UTILIZATION
2X THEORETICAL CYCLE TIME
0.5 DEFECTS PER CM2 AT 1 MICRON
100-150 mm WAFER SIZE
SEMICONDUCTOR MANUFACTURING in 2010

200 mm Wafer Diameter (8”)
Ballroom Facility Design
8,000 wafers per week
0.18 µm
5 levels metal, CMP
Cost of Plant $2 Billion
Equipment Reliability, Uptime Must be Maximized
100% Total Preventative Maintenance
Inter-Bay and Intra-Bay Automation
Advanced WIP Tracking to Eliminate Queues
Automated Tools and Recipe Handling
Extend the Useful Life of Tools
Hug the 100% Loading Capacity
TOMORROW’S SEMICONDUCTOR
MANUFACTURING TODAY

I.C. FACTORY COST $3 BILLION
BALLROOM, MINI-ENVIRONMENTS
300 mm WAFER DIAMETER (12”)
TOTAL AUTOMATION
GIGABIT DRAMS
150 MILLION TRANSISTOR I.C.’S
LESS THAN 0.045 MICRON FEATURES
LESS THAN 0.01 DEFECTS/CM²
2000 MHZ
2 BILLION INSTRUCTIONS/SEC
1.5 VOLT
1 INCH BY 1 INCH CHIPS
400 LEADS
25 WATTS/CHIP
NEW DESIGN TOOLS FOR BILLION TRANSISTOR CIRCUITS
CLEANROOM DESIGN

Ballroom Design

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SEMICONDUCTOR MANUFACTURING INCLUDES

FACTORY PROCESS FLOW

RIT p-well CMOS process flow, 60 steps, 9 photo steps, 7 oxide steps, 6 implants
Logistics, Ramp Up, Factory Floor Control, WIP Tracking

Thousands of wafers say 25,000 in the factory, what to do next. 300 products each with different mask sets for a total of 6000 masks to keep track of. 250,000 turns per day. 8000 wafer starts per week.
LOGISTICS

START

Access MESA Lot Status

LOT SELECTION RULES
- Do Photo first
- Do Oldest Lot Next
- Separate Lots
- Current Step
- Match Skill Level
- Use Equipment that is Up

Continue

Find Wafers

INITIAL QUALITY CHECK
- Count Wafers
- Check Picture Log Book
- Think
- Refer to Previous Process Step
- Check MESA Move-Out Comments

Preliminary Quality Check

On Hold?
- Yes
- See Lab Instructor
- No

On Hold?
- Yes
  - See Lab Instructor
- No

Mesa History Who Did Move-In

In Queue?
- No
- Find Queue Status
  - Step Number
  - Current Operation
  - Next Operation
  - Quantity
  - Apply Lot Selection Rules
  - Continue

In Queue?
- Yes

On Hold?
- Yes
  - See Lab Instructor
- No
  - Contact Person Determine What To Do Next
  - Final Quality Check
    - Pass?
      - Yes
        - Final Quality Check
          - Pass?
            - Yes
              - See Lab Instructor
              - No
            - No
              - See Lab Instructor
          - No
            - See Lab Instructor
        - No
          - See Lab Instructor

FINAL QUALITY CHECK
- Count Wafers
- Check Picture Log Book
- Think
- Do Results Make Sense?

Do Move-In Start Run Timer

Stop Run Timer Move Out Record Data

Clean Up Return Wafers Return Masks

END
CYCLE TIME MANAGEMENT

**CYCLE TIME** - the time it takes to process wafers from start to finish. Various cycle times can be calculated depending on the exact definition. Usually cycle time is the number of calendar days to process a lot from start to ship. Other variations include single wafer cycle times, cycle time based on work days rather than calendar, etc.

**BASELINE CYCLE TIME (work days), (BSWCT and BWLCT)** - this is the cycle time at the start of a cycle time improvement program. At that point in time a CIM system data base query is done to find the cycle time for each process flow (PMOS, NMOS, CMOS, EEPROM, etc.) This is used as the reference point for measuring cycle time improvement.
CYCLE TIME IMPROVEMENT

Cycle time, X factor
(times theoretical cycle time)

Fab 2 Cycle time

Ave

range

standard deviation

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Particle Count in Vicinity of Photoresist Spinner

Source: Donovan et al., 1988

Figure 9-7. Periodic bursts of particles larger than 10 nm in the vicinity of a photoresist spinner.
DEFECT DENSITY AND DIE YIELD

\[ \text{YIELD} = e^{-AD} \]

Where: \( A \) is the chip area (cm\(^2\)) and \( D \) is the density of defects (\#/cm\(^2\))

EXAMPLE: Chip Area is 1 cm\(^2\) and Defect density is 1/cm\(^2\)
\[ \text{YIELD} = e^{-1} = 37\% \]
YIELD AND MANUFACTURING

WAFER YIELD = \[\text{WAFER YIELD} / \text{STEP}\]^{\text{NUMBER OF STEPS}}

Example: \[\text{YIELD} = 98\%^{100} = 13\%\]

DIE YIELD = \text{NUMBER OF WORKING CHIPS/TOTAL NUMBER OF CHIPS}

Example: \[\text{DIE YIELD} = 52/61 = 85\%\]

COST OF DIE YIELD LOSS

= 5000 wafers/wk \times 52 \text{ wk/yr} \times \$5/\text{chip} \times 9\text{chips/wafer} = \$1.2 \text{ million/yr}
PROCESS INTEGRATION

PROCESS IS: A VARIETY OF SEQUENTIAL STEPS WHICH RESULTS IN HUNDREDS OF THOUSANDS OF TRANSISTORS BEING MADE AT THE SAME TIME ON EACH CHIP

UNIT PROCESSES ARE:
- DEPOSITION - CVD, LPCVC, PECVD, PVD
- SURFACE ALTERING - DIFFUSION, OXIDATION, ION IMPLANTATION
- PHOTOLITHOGRAPHY - G-LINE, I-LINE, EXCIMER LASER, X-RAY
- ETCHING - WET CHEMICAL ETCHING, PLASMA ETCHING, RIE
- CLEANING - RCA, MODIFIED RCA

PROCESS INTEGRATION: IS THE SEQUENCING THE UNIT PROCESSES INTO A SERIES OF STEPS THAT GIVES THE DESIRED RESULT
EVOLUTION OF MANUFACTURABILITY

- NEED FASTER CHIPS
- MORE FUNCTIONS
- PUSH FOR NEW PROCESS TECHNOLOGY
- INTRODUCTION TO MANUFACTURING
- MATURE PROCESS
- HIGH MANUFACTURABILITY
- PROCESS CAPABILITY IMPROVEMENT
- NEW PRODUCTS
- LOW MANUFACTURABILITY

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Technology is Transferred by People

Training Exchanges

Copy Exactly Attention to Detail Documentation
“you are not paid for coming to work. You are paid to make the product better”

TQM is a way to run a company that focuses on continually improving how you do what you do in order to satisfy all customer needs. TQM combines management methods and statistical tools in one package and gives all members of an organization a common goal.

Quality is defined as “conformance to customer requirements”, lack of defects and the companies own standards of final product.
CIM - Computer Integrated Manufacturing

CIM - Concept in which computer software and hardware is integrated throughout a manufacturing facility to provide integration among functions such as engineering and research, production planning, plant operations, shipping, receiving, business management, marketing, everything (including CAD and CAM).

CAD - Computer Aided Design, software and hardware tools needed to design the product including, circuit simulators, layout editors, process simulators, and more,

CAM - Computer Aided Manufacturing - software and hardware tools needed for work in process tracking, statistical process control, facilities monitoring, robotics, artificial intelligence, expert systems, and more.
COMPUTER AUTOMATED SEMICONDUCTOR MANUFACTURING

Process Engineering
CAD, CAM, SPC

START

Operation 1
Feed Back
Evaluate
Feed Forward

Operation 2

Operation N

Data Collection, Lot Control, Scheduling, SPC, Rework

Final Test

SHIP

Facilities, Equipment, Supplies
People, Training, Technical Support

Expert System
Robotics

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AUTOMATION

Workflow Automation:
People monitor and manage exceptions

Equipment Automation:
Hands-off processing

Process Automation:
Quality control based on machine data

Material Handling and Control Automation

Goal:
All execution and control fully automated
FULLY AUTOMATED 250,000 TIMES PER DAY

1. Processing finished
2. Data to SPC and R2R uploaded
3. Transport to next area started

SPC: Statistical Process control
R2R: Run-to-run

Metrology
Etch
Metrology

4. Lot for next tool reserved
5. Carrier transport to tool

6. Process parameter determined
7. Processing started
RUN TO RUN CONTROL

Measurement

Small fluctuations of processing

Lithography

Feed forward
Run-to-Run control

Parameter adjustment

Compensation of variations

Dry Etch

Feed back
Run-to-Run control

Parameter adjustment

Measurement

Small fluctuations of processing

Lithography

Feed forward
Run-to-Run control

Parameter adjustment

Compensation of variations

Dry Etch

Goal: Automatically minimize process variations
**RUN TO RUN CONTROL**

- Without R2R
- With Automated R2F

**SAMPLE_DATE**

- Manual updates using R2R
- With Automated R2F
SPC - STATISTICAL PROCESS CONTROL

§ CIM system integrated with SPC software - Quality Analyst
  § operators review SPC charts before processing
  § process adjustments can be made if necessary

§ SPC alarms and actions if process violates SPC rules:
  § send notice to specific users
  § prevent further processing of job, operation or tool

§ Corrective Actions

§ List of actions (flow chart) if SPC rules are violated
STATISTICAL PROCESS CONTROL (SPC)

Oxide Thickness, Å


USL

LSL

Date

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LITHOGRAPHIC ETCH CELL FORMATION

36 Possible Paths with cell formation
3 Possible Paths and less variation

Overall Variation
No Cells

Coat 1
Coat 2
Coat 3
Expose 1
Expose 2
Dev 1
Dev 2
Dev 3
Etch 1
Etch 2
SIX SIGMA CONCEPTS

Process Mean
off target

Process Variation
within specification
limits

Process Variation
larger than
specification limits

Mean

Target

LSL

USL

Mean

LSL

USL

Mean

LSL

USL

0

3σ

3σ

3σ

0

3σ

3σ

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Reduce Variation - locate $6\sigma$ points within USL and LSL & Position Mean at Target
Goal of $C_p=2.0$, $k=0$, $C_{pk}=2.0$ to give less than 3.4 ppm defects

\[
C_p = \frac{(USL - LSL)}{6 \sigma}, \\
K = \frac{[T_{get} - \mu]}{(USL - LSL)/2}, \\
C_{pk} = \text{Smallest of: } \left\{ \frac{(\mu - LSL)}{3 \sigma}; \frac{(USL - \mu)}{3 \sigma} \right\}
\]
DESIGN OF EXPERIMENTS (DOE)

Central Composite Designs

What can you measure?
- linear effects
- interactions
- quadratic effects

# factors | # runs
---|---
2 | 9
3 | 15
4 | 25
5 | 43
**Doe, Response Surface Analysis**

Model Equation: \[ F = 5X^2 - 1.5Y - 4XY + 12 \]

Surface Plot

Contour Plot

Tilt = 10° Rotation = 30°

(normalized response, X & Y in design units)

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COST OF OWNERSHIP (COO)

\[
\text{COO} = \frac{\$F + \$V + \$Y}{L \times \text{TPT} \times \text{Y(THP)} \times U}
\]

Where:
- \$COO is Cost of Ownership in $/wafer
- \$F is Fixed Cost
- \$V is Variable Cost
- L is Equipment Life
- TPT is Throughput rate
- Y(TPT) is Ideal Throughput Yields
- U is Utilization
- \$Y is Cost of Yield Loss
INDUSTRY NEED FOR HUMAN RESOURCES

The semiconductor industry is forecasted to grow even larger. Worldwide industry sales are projected to reach $400 billion by the year 2010. Most projections indicate that the semiconductor industry will need about 40,000 more skilled operators and technicians during the next five years and 8,000 semiconductor manufacturing engineers (Process Engineers, Product Engineers, Device Engineers, Defect Reduction and Yield Enhancement, Test Engineers, Reliability, Process Integration) in the next five years.
TYPICAL UNDERGRADUATE MICROELECTRONICS EXPERIENCE AT A UNIVERSITY

VLSI Design (or Digital Systems)
Analog IC Design (Electronics)
IC Technology
Semiconductor Device Fabrication Laboratory
Device Physics

All have very little Manufacturing Content
Approximately 1000 students/year
DESIGN

VLSI Design
VHDL
Analog IC Design
Circuit Simulation
Layout
Design Automation
Design Rule Checking
IC TECHNOLOGY

Oxidation
Diffusion
CVD/LPCVD/PECVD
Plasma Etch
Rapid Thermal Anneal
Physical Vapor Deposition
Ion Implant
Lithography
Technology Modeling
SEMICONDUCTOR DEVICES

- Electronics
  - Diodes, Transistors
  - Analog Building Blocks
- Physics of Semiconductors
  - MOS Structures
  - Transistors
- Microelectromechanical Devices
  - Sensors & Actuators
- Semiconductor Devices
  - CCD’s, CID’s
- Non-Silicon Devices
  - GaAs, III-V, II-VI
  - Flat Panel Displays
  - Liquid Crystal Devices
- Device Simulation
MICROLITHOGRAPHY

Exposure Tools, g-line, I-line, 248nm, 193nm, e-beam
Coat and Develop Tools
Resist Materials
  Positive Novalac Resists
  Negative Chemically Amplified
  Contrast Enhancement
  Dyed, ARC
  Multilayer
  Top Surface Imaging
  DUV, EUV, X-ray

Modeling
  Phase Shifting Masks
  DUV, EUV
Surface Analysis
SEM, TEM (EDAX)
AUGER, SIMS
XPS, ESCA

Materials Processing
Thin Films (metals, insulators)
CVD (LPCVD, PECVD, etc.)
Plasma Etching
Rapid Thermal Processing
Operations Research - Factory Floor Simulation, WIP Tracking, Cycle Time Management, Materials Resource Planning, Scheduling, Productive Maintenance


Statistical Process Control - DOE, Statistical Thinking, Time Series Analysis

Computer Automation - CAD, CAM, CIM, SECS I,II, Robotics, AI, Expert Systems
Most university IC labs exist to support research. Some are also used as educational IC labs. Sometimes separate IC labs are maintained for education.

The educational IC labs in universities exist to support courses in semiconductor technology, semiconductor devices, semiconductor manufacturing, microlithography and/or materials science.

Around 40 universities have IC lab facilities

About 15 universities have large complete facilities (> 10,000 sq.ft.)

Community Colleges are also starting programs to support the semiconductor industry and they are building educational facilities.
EDUCATIONAL LAB FACILITIES

BASIC
- 3-6 Tubes Furnace
- Resist Spinner
- Bake oven or Hot Plate
- Contact Printer/Aligner
- Wet Etch Hood
- Evaporator
- Optical Microscope
- 4pt. Probe
- Groove and Stain
- SUPREM II
- Manual Prober
- HP4145

CMOS CAPABLE
- Basic Facility
- Plus All Below:
  - LPCVD, Poly and Nitride
  - Wafer Coat/Develop System
  - Steppers
  - Plasma Etch or RIE
  - Sputtering
  - Ion Implant
  - SEM, Nanospec, Alphastep
  - SUPREM III, IV
  - PROLITH

ADVANCED
- CMOS Capable Facility
- Plus Some Of Below:
  - Maskmaking (e-beam or Optical)
  - CIM System
  - EDAX, AUGER, SIMS
  - XPS, ESCA
  - Packaging
  - Semi Automatic Probe and Test
  - MBE, MOCVD, RTP
These Universities have IC Fabrication Laboratory Facilities

Arizona State University  
Boise State University*  
Boston University  
Brown University  
Carnegie-Mellon University  
Case Western Reserve University  
Columbia University  
Cornell University*  
Duke University  
Florida Institute of Technology  
George Washington University  
Harvard University*  
James Madison University  
Massachusetts Institute of Technology*  
New Mexico State University  
North Carolina A&T University  
North Carolina State University*  
Northwestern University  
Pennsylvania State University  
Purdue University*  
Rensselaer Polytechnic Institute*  
Rochester Institute of Technology*  
Rutgers University  
Stanford University*  
San Jose State University  
Santa Clara State University  
Tufts University  
University of Arizona  
University of California at Berkeley*  
University of California at Santa Barbara  
University of California at Los Angeles  
University of Cincinnati  
University of Florida  
University of Illinois*  
University of Louisville  
University of Maryland  
University of Massachusetts  
University of Michigan*  
University of Minnesota*  
University of Mississippi

* Large IC Fabrication Facilities
These Community Colleges are developing programs to Prepare students for semiconductor manufacturing technology positions

Central Arizona College  Santa Fe Community College
Chandler/Gilbert Community College  Luna Vocational Technical Institute
Gateway Community College  SW Indian Polytechnic Institute
Glendale Community College  Dona Ana Community College
Mesa Community College  University of New Mexico Valencia Campus
Pima Community College  Chemeketa Community College
Mission College  Oregon Institute of Technology
Sna Jose City College  Portland Community College
Orange Coast College  Umpqua Community College
Pikes Peak Community College  Linn Benton Community College
Aims Community College  Austin Community College
Valencia Community College  Collin County Community College
Idaho State  Eastfield College
Southern Maine Technical College  Grayson College
Worcester Technical Institute  Mountain View College
Albuquerque TVI  North Central Texas College
Northern NM Community College  North Lake College
San Juan College  Richland College
Texas State Technical College-Harlingen  Tarrant County Junior College
Texas State Technical College-Sweetwater
Texas State Technical College-Waco
Weatherford College
Vermont Technical College
Centralia
Pierce College
Dallas County Community College
Collin County Community College
MICROELECTRONICS EDUCATION IN UNITED STATES UNIVERSITIES

Number of ABET Accredited EE Programs 250
Students in EE Programs 100,000 = 25,000/year
Students taking VLSI Design 5,000/year
Students in Fabrication Courses 1,000/year
Graduate Students Studying Semiconductors 2,400=300/year
Chemical Engineering Programs
  with Microelectronics Courses 10
Undergraduate Microelectronics Programs 10

RIT has the only ABET accredited BS program in Microelectronic Engineering
RIT PROGRAM

Started in the Fall of 1982
ABET Accredited
125 Undergraduate Students
15 Masters Students
5 Ph.D. Students
5 year Required Co-op Program for Undergraduates
Over 1000 Graduates

Addresses all Aspects of Microelectronics Manufacturing
Starting in the First Year
REFERENCES

5. EE Times, http://www.eetimes.com/
1. Look at all the references listed on the previous page.