Rapid Thermal Processing (RTP)

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OUTLINE

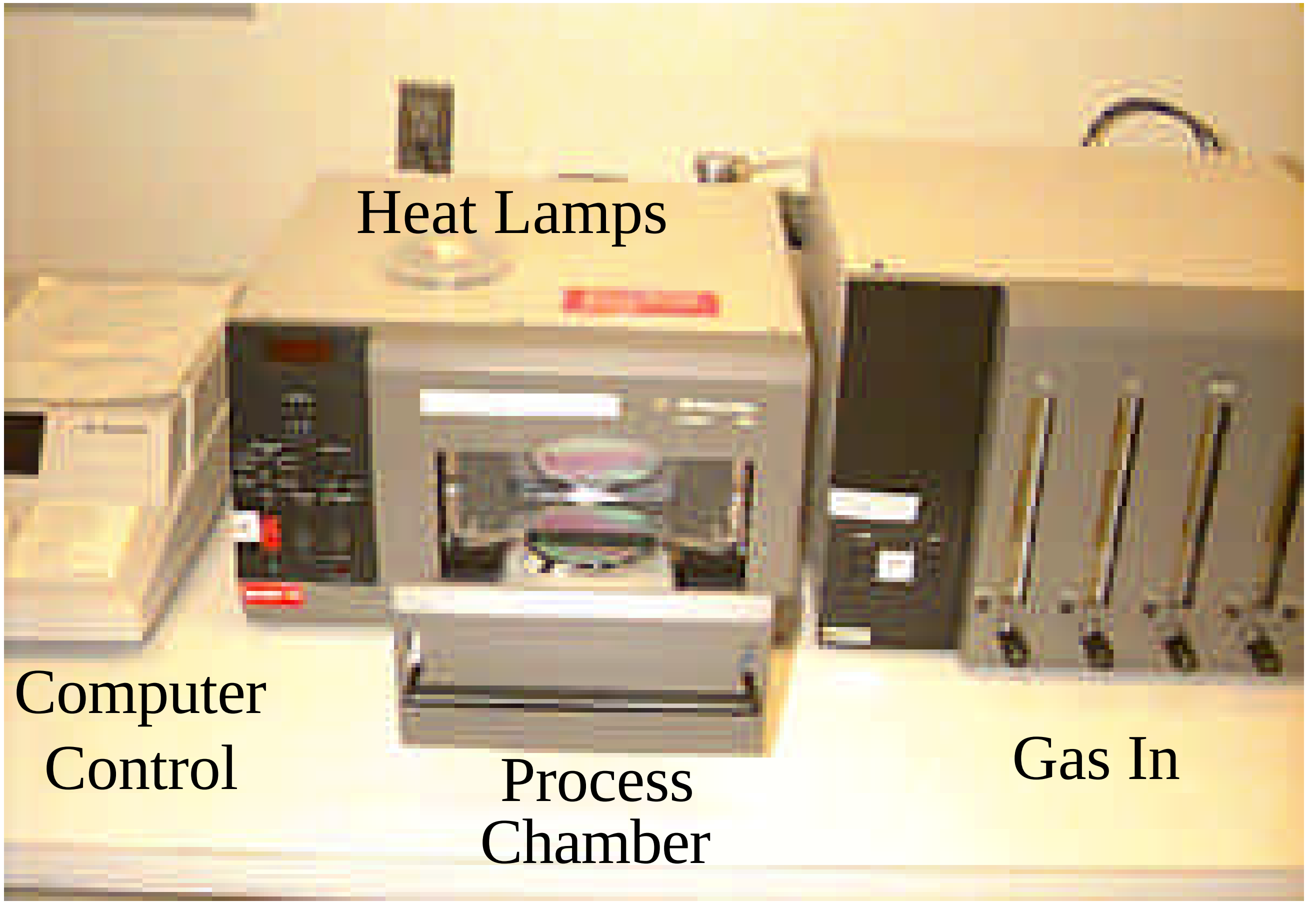
- Introduction
- Equipment
- Processes for:
    - Activation of Ion Implanted Impurities
    - Rapid Thermal Processing of Dielectrics
    - Silicidation and Contact Formation
- Thermoplastic Stress
- References

INTRODUCTION

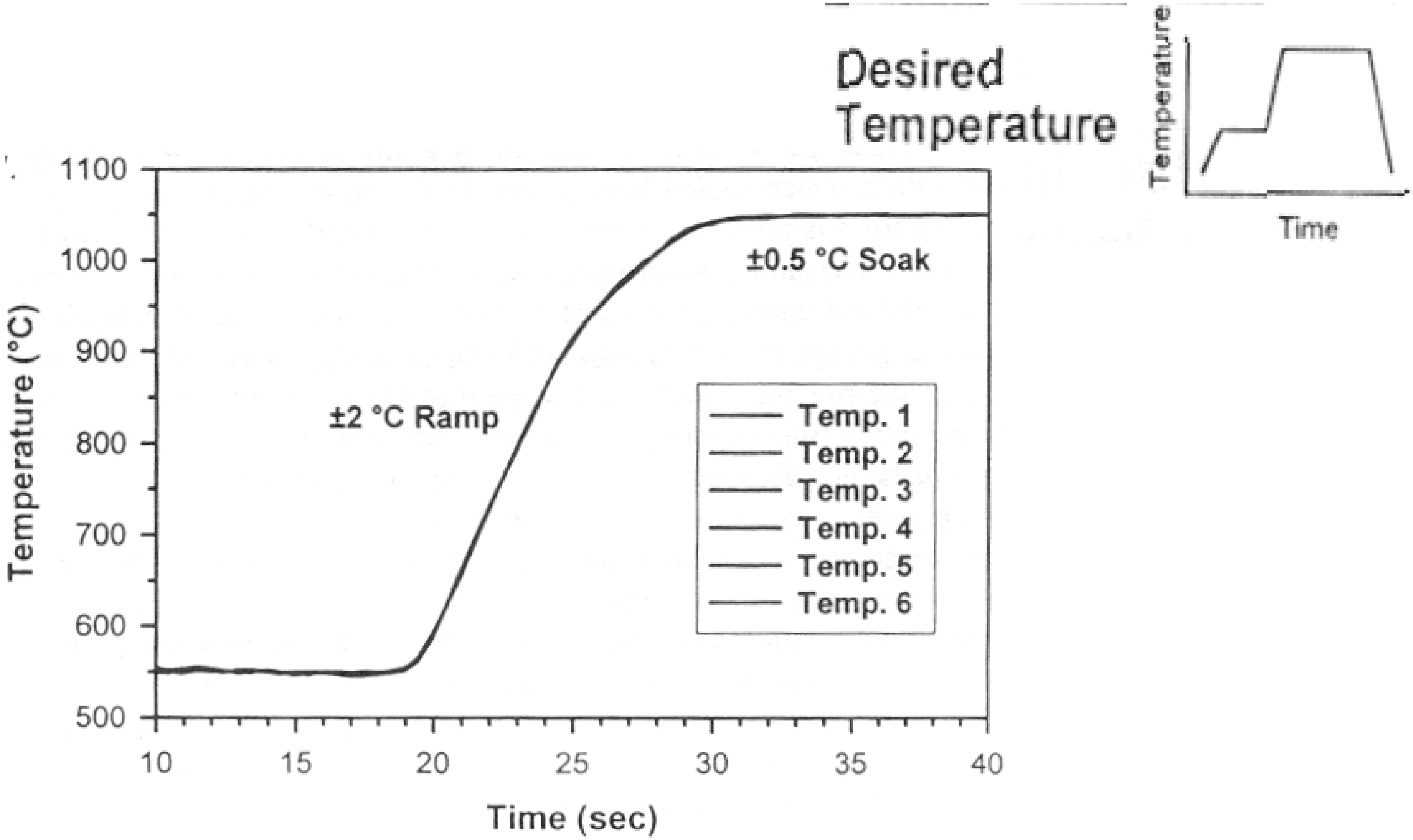
Rapid Thermal Processing (RTP) can be used to reduce the thermal redistribution of impurities at high temperature. For small devices this is an important consideration and as a result most engineers make use of low temperature processes. Some ion implants require high temperature (at least 1000 °C) thus RTP is a promising technology.

RTP was originally developed for ion implant anneal but has broadened its application to oxide growth, chemical vapor deposition, and silicidation.

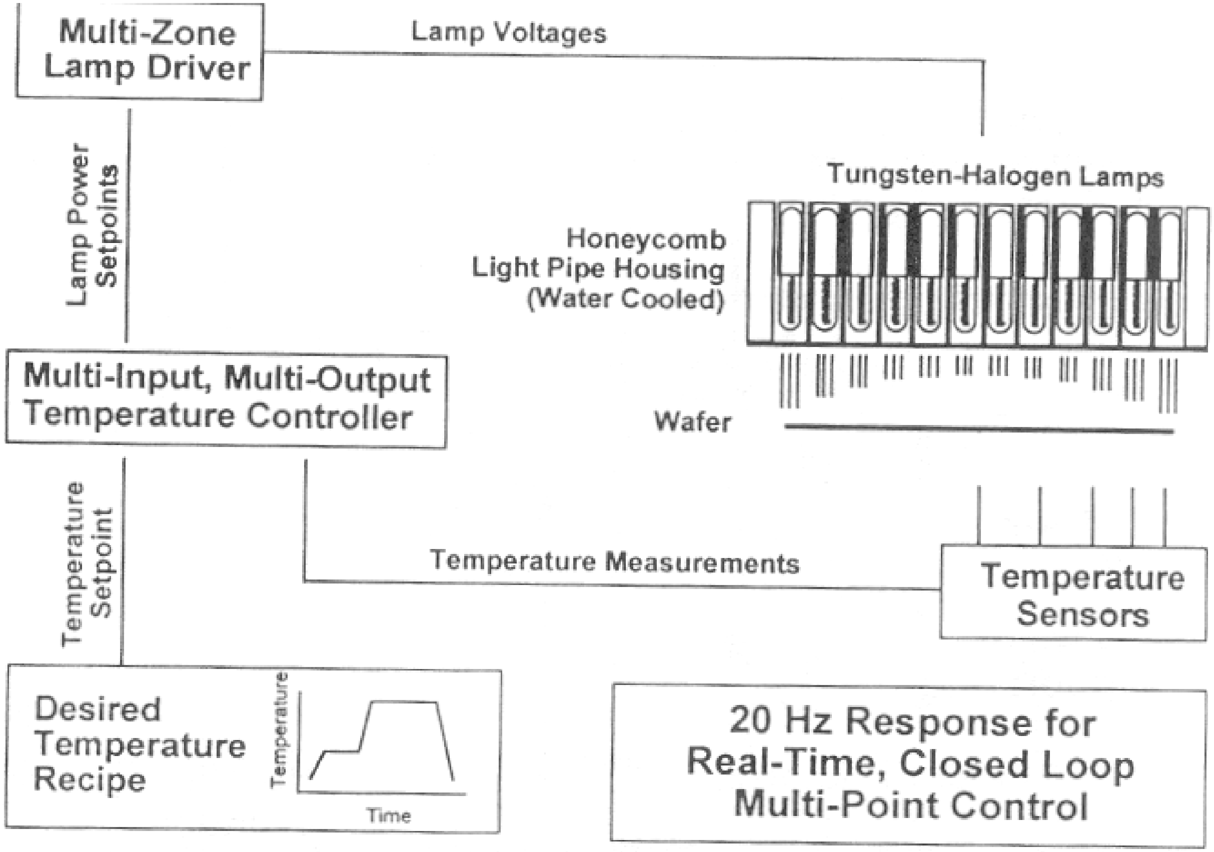
RAPID THERMAL PROCESSING (RTP)



RAPID TEMPERATURE RISE



RTP SYSTEM



ig. 8-28 Schematic of a closed-loop temperature control system. Courtesy of Applied Materials, Inc.

THIN GATE OXIDE GROWTH BY RAPID THERMAL PROCESSING (RTP)

From Textbook by S. Wolf

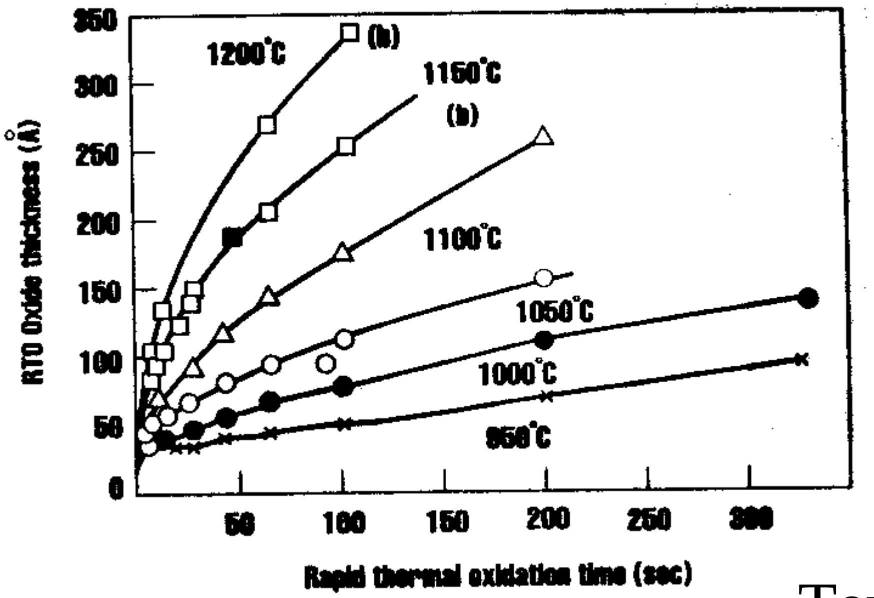
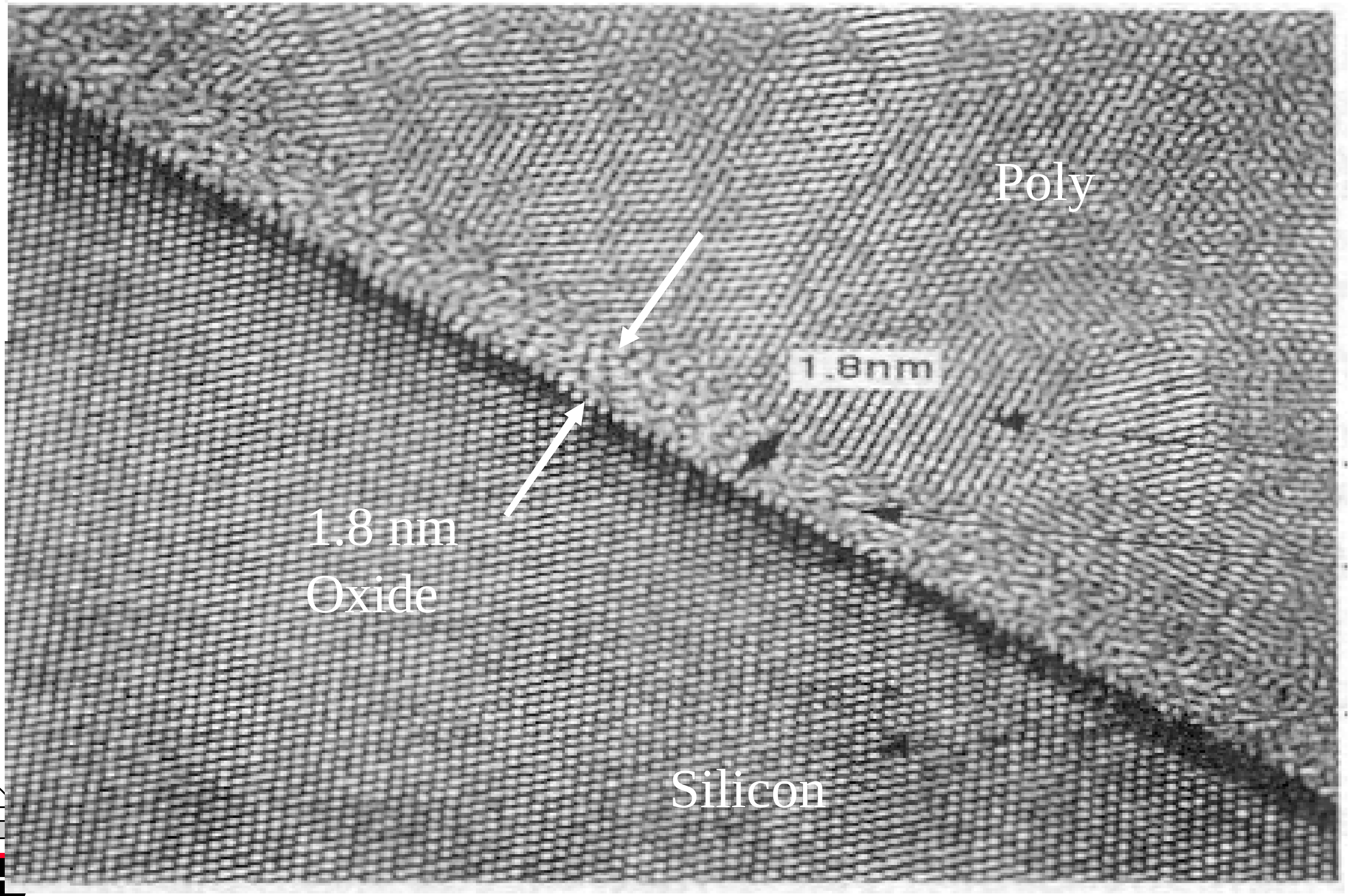


Figure 6-13 Typical data for oxide thickness as a function of time for a rapid thermal oxidation process (*after Moslehi et al., 1985*).


AG 610 at RIT

Textbooks say that 150Å of oxide can be grown by RTP at 1100°C in 60 sec.

RTP THIN OXIDE GROWTH



RTP RECIPE

Recipe for RTP Oxide, time during SS (Steady State) was changed to obtain different oxide thicknesses, 60s, 120s, 240s, and 480s

Step	Time (sec)	Temp (C)	T sw	Gain	Dgain	Iwarm	Icold
Delay	10						
Ramp	120	1000					
SS	10	1000	20	-250	-60	5500	5500
SS	480	1000	20	-250	-60	5500	5500
Delay	300						

Sébastien Michel, February 2005
Steve Parshall, Kazuya Tokunaga, May 2005

OXIDE THICKNESS MEASUREMENTS

The data shown was obtained using the 5 point 6”wafer Spectromap

RTP Oxide at 1000 C, Dry O2

Time	8	4	2	1	Min.
Mean	211.53	150.13	104.29	67.04	A
Max	271.26	174.22	132.36	71.245	A
Min	167.06	130.35	57.249	53.866	A
STDDEV	37.112	20.187	28.929	14.234	%
Center Pt	271.26	174.22	132.36	71.245	A

The data shown was obtained using the VASE (Variable Angle Spectroscopic Ellipsometer)

Time	8	4	2	1	Min
Xox	272.54	167.59	143.03	55.77	A
n	1.45	1.45	1.45	1.42	

RTP OXIDE QUALITY MEASUREMENTS

Measurements made using the SCA (Surface Charge Analyzer)

Time	8 minutes	4 minutes	2 minutes	1 minute
NSC	1.13E+14	1.64E+14	1.46E+14	7.56E+14
Qox	3.55E+11	4.26E+11	4.28E+11	4.73E+11
Dit	2.76E+11	3.05E+11	4.32E+11	4.13E+11
Qfb	4.66E+11	5.53E+11	5.94E+11	7.05E+11
Ts	83	78	126	151

Dit is close to Bruce Furnace thermal gate oxide values
Typically ~1E11

ULTRA SHALLOW JUNCTION FORMATION

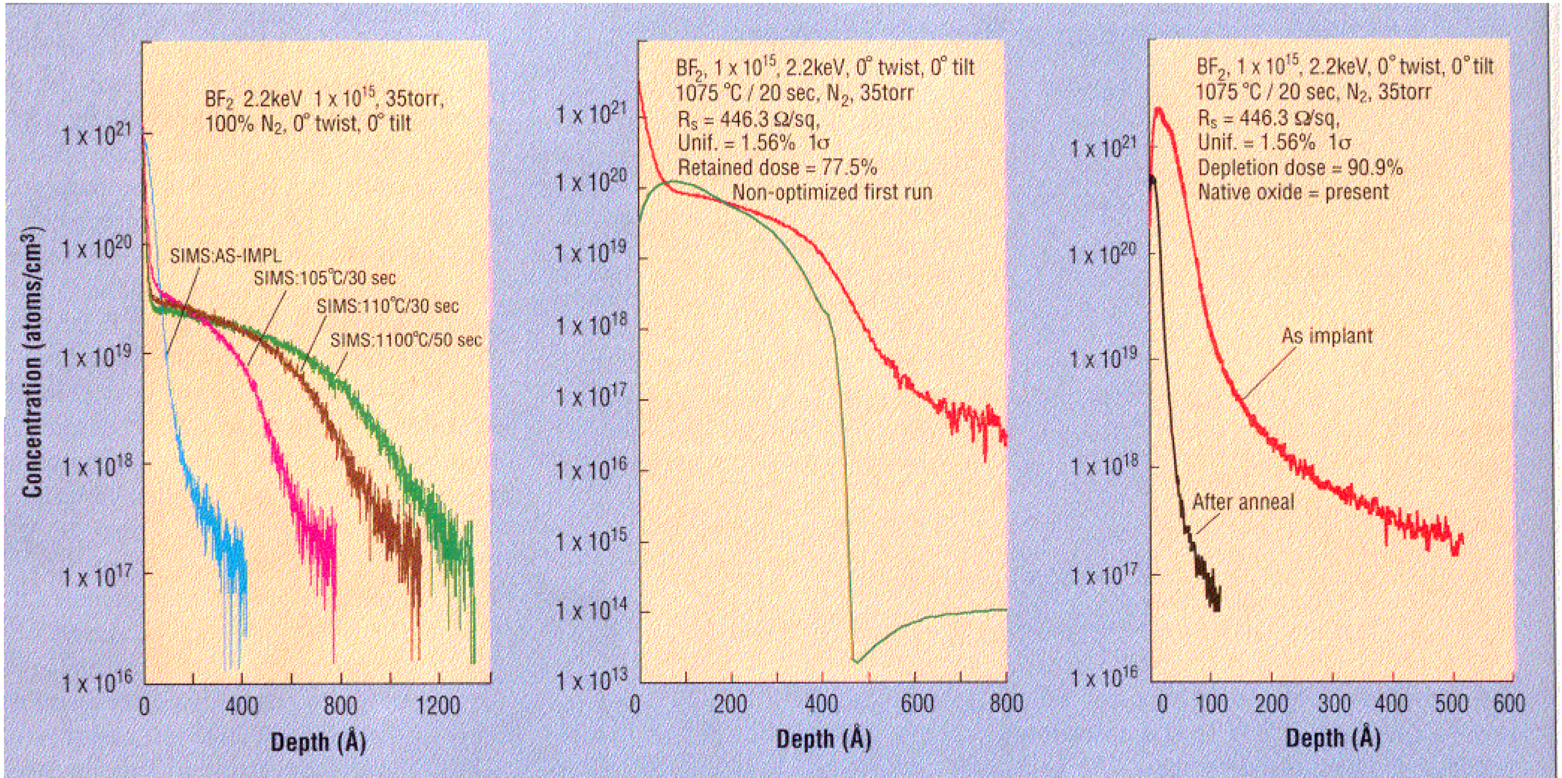


Figure 4. (Left) Concentration profiles (measured via SIMS) for 2.2keV, BF$_2^+$, 1 × 10^{15}/cm^2 implants using 30-sec and 50-sec processes. **Figure 5.** (Center) Concentration profiles (measured via SIMS and SRP) for 2.2keV, BF$_2^+$, 1 × 10^{15}/cm^2 implants using a 1075°C/20-sec process. **Figure 6.** (Right) Fluorine depletion before and after anneal.

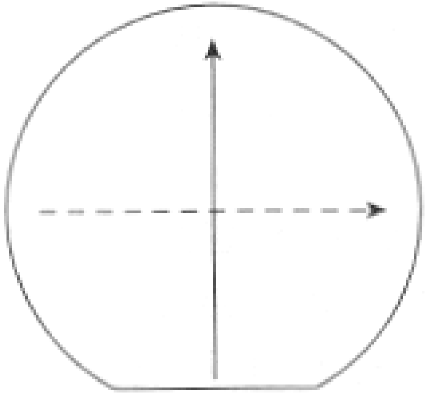
SILICIDE AND BARRIER LAYER FORMATION

Silicide formation includes Ti, Pt, W, Ta, Mo, and Co. $TiSi_2$ is formed at 900 C in pure N_2. Titanium is sensitive to H_2O and O_2 in the ppm levels.

TiN barrier layers can be formed by reacting Ti with N_2 or NH_3

ILLUMINATION UNIFORMITY AND WAFER TEMPERATURE UNIFORMITY

Uniformity of temperature across the wafer is the most important parameter. Local across the wafer temperature gradients cause stress.



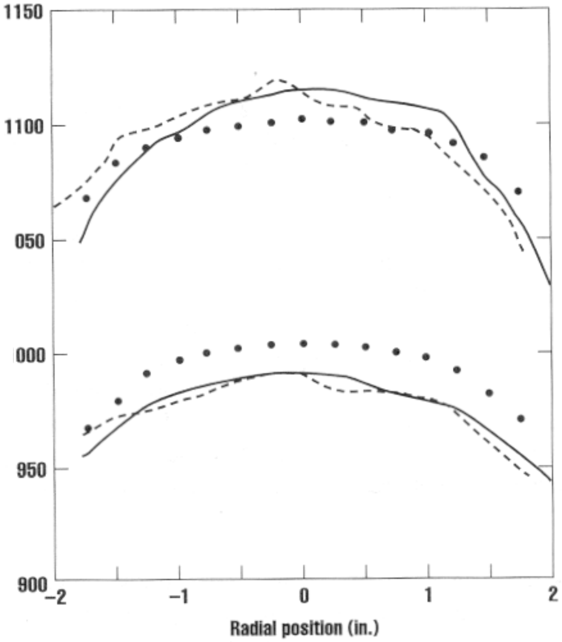


Figure 6-6 Typical wafer temperature distributions across the wafer in an early generation rapid thermal system (*after Lord, ©1988 IEEE*).

LAMP-BASED RTP

Lamp based RTP systems have been the choice for the past several years. Special physical configurations have used to provide additional heat towards the outer edge of a round wafer. These systems are cold wall systems so more power is needed at the wafer edge than in the center of the wafer.

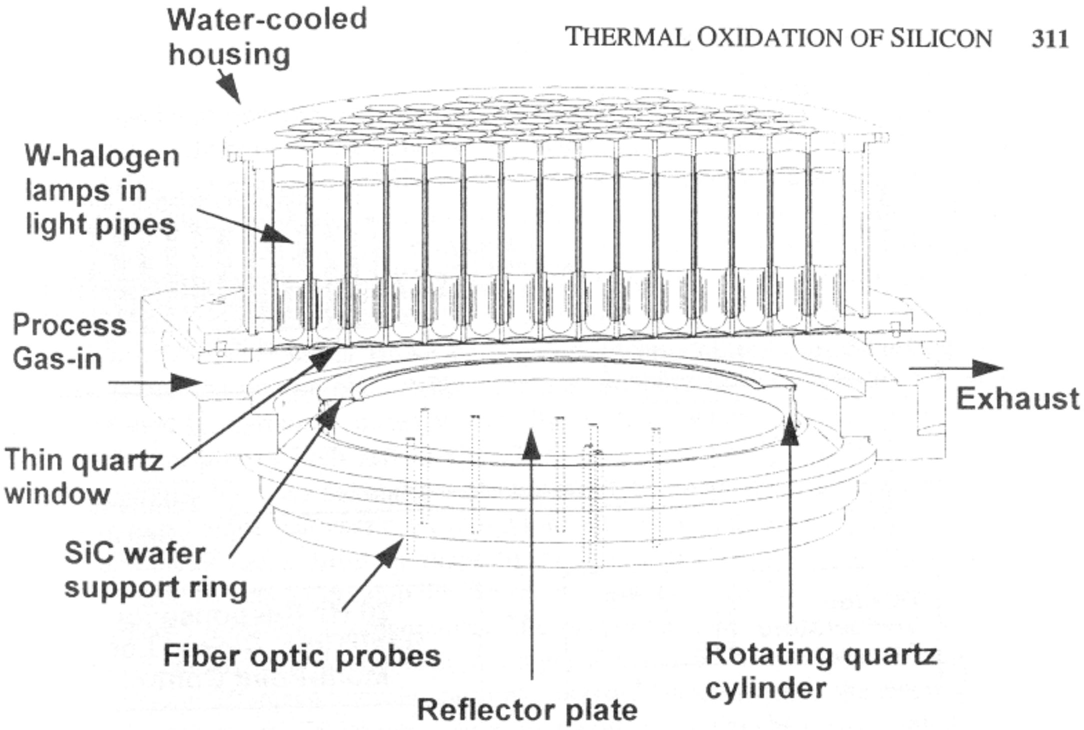


Fig. 8-27 Schematic cross-section of a rapid-thermal processor. Courtesy of Applied Materials, Inc.

SUSCEPTOR BASED RTP SYSTEM

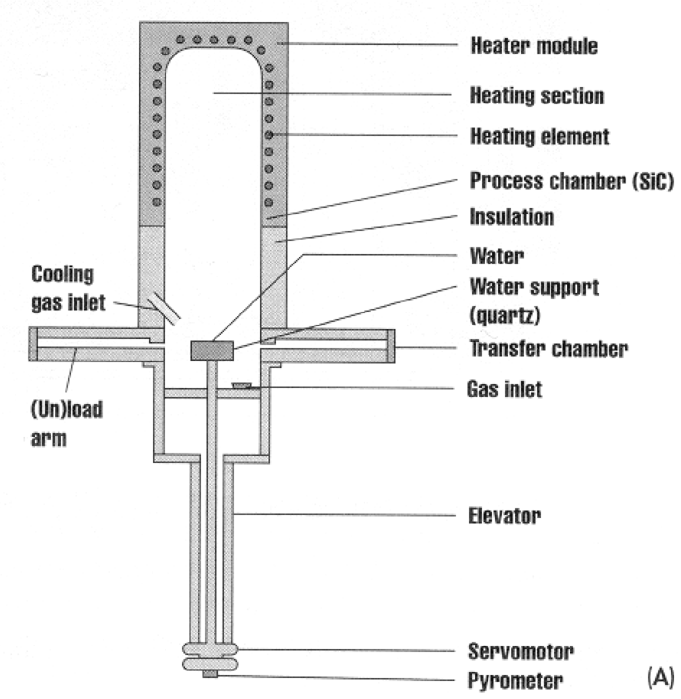


Figure 6-15 New designs for high uniformity RTP include: (a) the hot wall system (after Roozeboom and Parekh), (b) the multizone hexagonal system (*after Cho et al.*), and (c) the multizone cylindrical system (*after Moslehi et al., 1991, used with permission of Materials Research Society*).

In the susceptor-based, hot-wall system, heating is achieved by placing wafers in close proximity to a heated thermal mass and thereby heating the wafers with a uniform flux of relatively long wavelength radiation. In such a system, the initial temperature ramp-up rate increases with increase in process temperature. Heat-up and cool-down rates in excess of 100 °C/sec.

TITANIUM SILICIDE FORMATION RECIPES

FACTISI1.RCP (step 1 – form TiSi)

Delay 30 sec.
Ramp 75 °C/sec. To 650°C
Steady State 60 sec.at 650°C
Ramp 125°C/sec. To 300°C

Etching of Ti Metal (step 2)

Heat the Sulfuric Acid:Hydrogen Peroxide (1:2) mixture on a hotplate to 100°C (set plate temperature to 150°C)

Etch for 1 min 30 sec. This should remove the Ti that is on top of the silicon dioxide but not remove TiSi that was formed on the polysilicon and D/S regions. It also removes unreacted Ti metal over the TiSi on the poly and D/S regions.

FACTISI2.RCP (step 3 – form $TiSi_2$)

Delay 30 sec.
Ramp 75 °C/sec. To 800°C
Steady State 60 sec. At 800°C
Ramp 125°C/sec. To 300°C

SUMMARY

Rapid thermal processing was developed to enable short time high temperature implant annealing. Generally, the wafer rests on quartz pins in a flow tube and is heated using a bank of high intensity filament lamps.

Problems with RTP include temperature measurement and thermal uniformity of the wafer. Excessive temperature gradients across the wafer cause thermoplastic stress that may lead to wafer warpage and/or slip. Rapid thermal processing has been extended to include silicide and barrier metal formation, thermal oxidation, chemical vapor deposition, and epitaxial growth.

REFERENCES

1. “The Science and Engineering of Microelectronic Fabrication”, Stephen A. Campbell, Oxford University Press, 1996.

HOMEWORK - RTP

1. Describe the application of RTP for ion implant anneal.
2. Discuss why RTP would be good for gate oxide growth.