1. You are to add support for the jr (jump register) MIPS instruction to the MIPS single-cycle datapath of figure 5.17 (page 307).
   a) Add necessary datapath components, connections, and control signals to support this instruction. **Justify the need for the modifications.**
   b) Specify control line values for this instruction by adding a new row for jr to the control table in Figure 5.18 (page 308).

2. You are to add support for a new instruction l_inc (load increment) to the MIPS single-cycle datapath of figure 5.17 (page 307). The l_inc instruction is a variant of lw (load word) which increments the base address register after loading from memory. This instruction (l_inc) corresponds to the following two instructions:

   \[
   \begin{align*}
   &\text{l}w \ $r_t, \ L($rs) \\
   &\text{addi} \ $rs, \ $rs, \ 4
   \end{align*}
   \]

   Where L is just the usual offset. You may assume that register specifiers $rs, $rt do not refer to the same register.
   a) Add necessary datapath components, connections, and control signals to support this instruction. **Justify the need for the modifications.**
   b) Specify control line values for this instruction by adding a new row for l_inc to the control table in Figure 5.18 (page 308).
   c) Explain why it is not possible to modify the single-cycle datapath to support the l_inc instruction without modifying the register file.
3. You are to add support for the lui (load upper immediate) MIPS instruction to the MIPS multicycle datapath of Figure 5.28 (page 323). Provide a solution that completes this instruction in 3 cycles.
   a) Add necessary datapath components, connections, and control signals to support this instruction. **Justify the need for the modifications.**
   b) Show the necessary modifications to the multicycle control finite state machine of Figure 5.37 (page 338) to support the lui instruction. In addition to relevant control line values, you must provide dependant RTN statements for each state you add.

4. You are to add support for a new instruction ldi (load immediate) to the MIPS multicycle datapath of Figure 5.28 (page 323). This instruction (ldi) loads a 32-bit immediate value from the memory location following the instruction into register rt.
   a) Add necessary datapath components, connections, and control signals to support this instruction. **Justify the need for the modifications.**
   b) Show the necessary modifications to the multicycle control finite state machine of Figure 5.37 (page 338) to support the ldi instruction. In addition to relevant control line values, you must provide dependant RTN statements for each state you add.

5. Consider a change to the MIPS multicycle datapath that alters the register file so that it has only one read port.
   a) Describe and also illustrate (via a diagram) any additional changes that will need to be made to the datapath (Figure 5.28, page 323) in order to support this modification.
   b) Modify the finite state machine (Figure 5.37, page 338) to indicate how the instructions will work given the modified datapath.

You can photocopy the figures or use versions from lecture notes to make it faster to show needed modifications.