Chemical Mechanical Planarization
For MEMS

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**CMP**

**Chemical Mechanical Planarization**
Polishing for the purpose of planarizing integrated circuit structures, and other microelectronic devices.

**Chemical Mechanical Polishing**
Includes traditional polishing, eg. Optics, semiconductor wafer preparation, metals
Introduction
What do we mean “to planarize” an IC?
Why do we need to planarize?
Are there other ways to planarize?
Principles of polishing and planarization
References
Homework
Six levels aluminum interconnect with tungsten plugs, CMP, and damascene of local tungsten interconnect for 0.18 µm gates.
§ CMP

• To flatten the surface of an integrated circuit by using a polishing process, i.e., by rubbing with a pad and slurry to remove the high regions of the circuit.

• High regions on the circuit should be removed by an equal amount, regardless of their area. Removal should be uniform across the whole wafer (many circuits).

• Removal must occur without causing damage to the circuit, or the wafer.
WHAT TO WE MEAN, TO “PLANARIZE AN INTEGRATED CIRCUIT”?

Planarization is one or both of the following:

a. Topography smoothing:
   the conversion of abrupt, vertical steps to gradually sloping transitions.

b. Step height reduction:
   the reduction of elevation differences
SMOOTHING VS. STEP HEIGHT REDUCTION

Unplanarized Step

Smoothing, no step height reduction.

Smoothing, with step height reduction.

Degree of Planarization  = 1 − \frac{h_2}{h_1}
PLANARIZATION RANGE

Short Range: \( r = 1 - 2 \ \mu m \)
\( \theta = 30 - 45 \ \text{deg.} \)

Long Range: \( r = 100 - 200 \ \mu m \)
\( \theta = 1 - 0.01 \ \text{deg.} \)

Global Planarization

\[
\text{Planarization Range (r)} = \frac{\text{Post-Step Height}}{\tan (\theta)}
\]
WHY DO WE NEED TO PLANARIZE?

Lithography is better with planar surfaces. Higher resolution is possible. Small depth of focus problems can be avoided.

Shallow trench isolation in CMOS processes.

Multilayer metal.

Patterning materials that are hard to etch.

Some MEMS devices will not move unless they are flat. Especially gears and linkages.
i-Line Stepper $\lambda = 365 \text{ nm}$
$NA = 0.52, \sigma = 0.6$
Resolution = $0.7 \lambda / NA = \sim 0.5 \mu m$
20 x 20 mm Field Size
Depth of Focus = $k_2 \lambda/(NA)^2$
**RESOLUTION AND DEPTH OF FOCUS**

§ Resolvable Linewidth = $k_1 \frac{\lambda}{NA}$

§ Depth of Focus = $k_2 \frac{\lambda}{(NA)^2}$

\[\lambda = \text{exposure wavelength (365 nm)}\]
\[NA = \text{numerical aperture of stepper (0.52)}\]
\[k = \text{constant, whose value depends strongly on the resist system and type of feature (0.61 theoretical)}\]

§ For resolution of ~0.5 µm, depth of focus is ~0.8 µm, therefore planarization is required.
SHALLOW TRENCH ISOLATION (FEOL)

1. Thermal Oxidation Deposit Nitride

2. Pattern and etch Nitride and oxide

3. Etch trench in silicon substrate

4. Thermal Oxidation Deposit CVD Oxide

5. CMP of oxide to Nitride polish stop

6. Chemical strip of Nitride

Nitride polish stop and its subsequent removal helps to minimize dishing in trenches.

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CROSS SECTION OF MULTI LAYER METAL STRUCTURE PLANARIZED BY CMP

 CMP Steps

 Thermal Oxide

 Silicon Wafer

 CMP

 Oxide

 M-1

 M-2

 M-3

 ILD 0

 ILD 1

 ILD 2

 W plug

 Ti/TiN Barrier

 Polysilicon gate

 BPSG
CMP IN MEMS ALLOWS DEVICES TO MOVE (SPIN)

X and Y movement
90° out of phase

Poly 1 – rotating gear
Poly 2 – anchor pin
Poly 3 – linkage

Poly 1 – X/Y motion

Where is CMP used and why?
CMOS FIRST MEMS AFTER, TEXAS INSTRUMENTS

TI Digital Mirror Array

TORSIONAL MIRRORS

1 million Mirrors
Buried Polysilicon MEMs with CMP planarization and CMOS post-fabrication (after Nasby, et al, 1996)
WHAT IS PLANARIZED, SPECIFICALLY?

§ **Front end Applications** (FEOL) - Devices in the active regions of the silicon wafer, such as:
   - Shallow trench isolation (STI)
   - Trench capacitors
   - Inter-polysilicon dielectrics

§ **Back end applications** (BEOL) - Metal and dielectric films which comprise the wiring of the millions of devices in the silicon wafer.
   - Pre-metal dielectrics (doped oxides, e.g. BPSG, PSG)
   - Lateral and Vertical interconnections (Al, W, Cu, Ta, Ti, TiN, doped Silicon Cu-alloys, Al-alloys)
   - Intermetal dielectrics (TEOS, SOG, SiO₂, BPSG, PSG, Si₃N₄)
   - Polymers (Polyimide)
OTHER METHODS OF PLANARIZATION

§ Thermal flow
§ CVD and Reflow
§ RIE Etchback of sacrificial layer
§ Spin-on-glass (SOG)
§ Variations of above
WHY IS CMP SO GREAT?

§ It is the only process which can planarize on a global scale.
  § Alternative planarization processes are affected by the pattern size and density.

§ It is an enabling process:
  § Maximizes lithographic performance.
  § Improves cleaning.
  § Reduces yield limiting defects from other processes.
  § Permits the use of difficult-to-etch metals such as Cu.
WHAT IS LAPPING and POLISHING?

Lapping –
To planarize or to create desired shape or dimension.
To produce a uniformly abraded surface with known degree of sub-surface damage (~1/4 of grit size)
Slurry of water and 8-micrometer alumina grit.
Cast iron lapping plates, double side lapping produces flatness and parallelism < 2 µm.
Typical removal, 50 µm per side.

Polishing –
To remove residual damage from lapping
To produce no new damage
To create a microscopically smooth surface
Does not change the shape of the surface
Gentle rubbing with a soft pad saturated with polishing slurry (CeO2, Fe2O3, ZrO2, SiO2). It involves both a chemical and a mechanical component. At pH=10.5
Wafers are often thinned before packaging. A thinner wafer allows for better heat removal, lower electrical resistance through the substrate and thinner packages. In MEMS wafer thinning allows for easier formation of thru wafer holes when combined with CMP double sided processing. We have been thinning our MEMS wafers from ~500µm down to ~300µm and then polishing to make thin double sided starting wafers.
SILICON POLISHING VS IC PLANARIZATION

**POLISHING**
- Subsurface damage
- Lapped surface
- Pad
- Monocrystalline silicon

**PLANARIZATION**
- Device region
- Pad
- Patterned surface, Pad may contact two materials.
- Metal
- Oxide
- Silicon

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Pad saturated with slurry.
Polishing pressure greatest on small, elevated features (active).
Pad may contact larger low areas (large field regions) called dishing.
**ELECTROMET GRINDING TOOL**

Platen Speed = 200 rpm  
Pressure = 40 psi  
Removal Rate = ~6 min/100µm  
Time = 12 min  
Water On

Grinder

Wafer Thickness Measurement

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GRINDING DISK

PSA Disc, Dia 8 In, 800 Grit, Diamond Abrasive, For Use With Orbital Sanders or Vertical Shaft Grinders with PSA Back-Up Pads, For Grinding Glass


Grinding Disk
Strassbaugh CMP Tool

Slurry: Klebosol 1501-50 Colloidal Silica 5 gal pail
$255 each, Mfg AZ Electronic Materials, Clariant’s Klebosol line of silica slurries, 50nm particles, KOH, pH 10.9, 50% solids or equivalent slurry.

15 min per wafer
Slurry drip rate: ~1 drop/second
Down Pressure = 8 psi
Quill Speed = 70 rpm
Oscillation Speed = 6 per min
Table Speed = 50 rpm (~10 Hz)
CMP TOOL MANUFACTURERS

- Applied Materials
- Cranfield Precision
- Ebara
- Fujikoshi
- Lapmaster
- Mitsubishi
- Nutool
- Okimoto
- Peter Wolters
- Presi
- Sony
- Speedfam/IPEC
- Strasbaugh
- Toshiba
SLURRY DISTRIBUTION SYSTEMS

Chemical Room

Polish Room

Slurry Distribution System

Polish Slurry 1250-liter Daytank

Mixer and Distribution

Slurry Concentrate 200-liter Drum

Ebara
FSI
Mega Systems
Speedfam/IPEC
Systems Chemistry
Universal Photronics
POST CMP CLEAN TOOLS

Tools
Dai Mippon Screen (DNS)
Oliver Design
OnTrak Systems (Lamb)
Solid State Equipment
Speedfam/IPEC
Sumitomo Metals
Toshiba

PVA Brush Rollers
Cupps Industrial
Kanebo
Merocel
Syntax
Universal Photronics
Right now we don't have a good way to measure the wafer thickness. Just the mechanical dial micrometer shown. But that shows less than 1 mil (25µm) change across wafer diameter.
We used our long scan Tencore P2 profiler to see if that will give us a better idea of the uniformity of these processes.

Surface roughness ~1µm (10,000Å) after grinding  
After polish ~50Å
**OPTICAL METROLOGY TOOLS**

- ADE
- Bio-Rad
- Mamamatsu
- Hitachi
- Horiba
- KLA/Tencor
- Matec
- Nanometrics
- Rudolph Instruments
- Speedfam/IPEC
- Topcon

Diagram:

- **MONOCHROMATOR & DETECTOR**
- **WHITE LIGHT SOURCE**
- **OPTICS**
- **WAFER**
- **3000 Å OXIDE**

- White light source
- Monochromator & detector
- Optics
- Wafers
- 3000 Å oxide layer
Impregnated – non woven polyester base, saturated with polyurethane which binds the base together when cured. Pad is abrasively buffed to condition it for use. Range of hardness and densities are available.

Cast – foamed polyurethane is cast in molds and cross-linked, after which it is sliced into sheets from 0.020 to 1.25 inches thickness. A wide range of density and hardness is available.

Coated – a non woven polyester base is coated with a polyurethante formulation which forms a skin layer which is abrasively buffed before use. Often used as a final cosmetic polish after stock removal with cast or impregnated pads.
PADS

3M
Cabot
Freudenberg
Fujibo
Kanebo
Rodel
Teijin Mills
Universal Photonics
STACKED PAD

Hard top pad

Resilient bottom pad

Metal platen

Hard upper pad reduces dishing while compressible lower pad conforms globally to the wafer surface, improving uniformity.
PAD CONDITIONING

Purpose
- to help maintain stability of removal rate in CMP
- To maintain long pad life
- To maintain removal rate uniformity within wafer
- Removes imbedded and caked debris in pad surface
- Exposes uniform pad material
- Abrades pad surface
- Maintains planar pad surface

Technique
- A diamond plated disc is applied to the pad using a prescribed downward force and rotation program, in the presence of water
**SLURRIES**

**Metals**
Colloidal alumina and ferric nitrate, low pH

Weak oxide film is formed using MnO2 based polishing agent, which is removed with MnO2 mechanical action.

**Oxides**
Colloidal Silica (sub micron particle size) in water with KOH or NH4OH, pH of 10.5

Cerium Oxide CeO2 (sub micron particle size), High Ph

Zirconium oxide
SLURRY MANUFACTURERS

Cabot
EKC Technologies
Fujimi
Intersurface Dynamics
Praxair
Rodel
Transelco/Ferro
Universal Photonics
COMPARISON BETWEEN OLD CMP SLURRY AND PROCESS AND NEW SLURRY AND PROCESS

Old Process and Slurry

Wafer before CMP

After 5 minutes of Polishing
Center not done

After 9.5 minutes of Polishing
Center done, Edges Bare

New Process and Slurry

After 2.25 minutes of Polishing
Clear almost every die
Even edge die
NEW RIT CMOS FACTORY STI PROCESS

- Carrier speed: 30 RPM
- Platen speed: 100 RPM
- Without back pressure
- 8 PSI down force (36 PSI on the gauge)
- Slurry (made for STI, see pages below)
- Slurry flow rate (60 mL/min)
- Pad conditioning: before every run
- Temperature: 80°C
- Polishing time: 2min 30 sec for 6500A oxide

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Eminess Technologies, Inc.
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Tempe, AZ 85282
Tel (408)505-3409, 888-899-1942,
fax (480)951-3842

Darlene Werkmeister
Dwerkmeister@eminess.com

1/05/06 Order:
N-2350-P Nalco 2350, 5 gal pail $166 each, Mfg by Rohm and Haas,
Silica, 70-100nm particle size, weight % 28, KOH, pH 11.4-12.4

R-10027556 Klebosol 1501-50 Colloidal Silica 5 gal pail $255 each,
Mfg AZ Electronic Materials, Clariant’s Klebosol line of silica
slurries,50nm particles, KOH pH 10.9 50% solids

R-10087555 EXP CELEXIS CX94S Single Component Slurry, 20Liter pail $235
each, Mfg by Rohm and Haas Ceria 20nm particles, STI, pH ~7

http://www.EMINESS.com
http://www.electronicmaterials.rohmhaas.com
CONVENTIONAL PROCESSING TECHNOLOGY FOR MULTILEVEL METALLIZATION

1. Deposit and pattern metal for via plugs

2. Deposit insulating film

3. CMP insulating film

4. Repeat steps 2-5 for next level (metal lines)
INLAID METAL (DAMASCENE) TECHNOLOGY

1. Previous metal lines
   Previous metal vias

2. Deposit Dielectric and etch vias

3. Deposit blanket metal

4. CMP metal

5. Repeat steps 2-5 for next level of metal lines.
**DUAL INLAID METAL (DUAL DAMASCENE)**

1. Deposit insulator, cap with nitride etch stop. Pattern nitride for studs, deposit second layer of insulator, apply resist.

2. Etch insulator down to substrate, strip resist.

3. Deposit metal, filling all features.

4. CMP of metal, stop at dielectric.

Dual approach requires 20-30% fewer steps than traditional subtractive patterning.
• Corrosion of the metal by the slurry (chemical)
• Passivation (self-limiting corrosion due to surface protective layer, usually oxide)
• Removal of the passivation from the high regions, from the action of the pad/slurry attrition.
• Reformation of the passivation layer on the exposed metal surfaces.
Cu INTERCONNECT

METAL 2 (Cu)

W PLUGS

METAL 1 (W)
PRESTON’S EQUATION

Removal rate is proportional to pressure and velocity:

\[ R \propto S \frac{F}{A} \quad \text{Or:} \quad R = K_p S \frac{F}{A} \]

in which:
- \( R \) = removal rate
- \( S \) = relative velocity
- \( F \) = Force on work piece
- \( A \) = area in contact with pad.
- \( K_p \) = Preston coefficient

Volume removal: \( RA = K_p S F \)

Many polishing processes obey this relationship fairly well, however it ignores any chemical effects.

Preston, F., (1927)

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**POLISH RATE VS. PATTERN DENSITY**

Volumetric rate: $RA = Kp F S$

- **Blanket Polishing**
  - Area = Wafer area
  - No pad contact between features

- **Patterned polishing**
  - Area = pattern area
  - Some pad contact between features.
  - Area = ?

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We have made great progress in doing the CMP for our advanced CMOS process shallow trench isolation (STI). The progress has been made through:

1. Getting the Westech CMP tool working correctly.
2. Getting a slurry especially made for STI that removes oxide and stops on nitride.
3. Adding tiles (dummy features) to the mask area outside of the active regions during computer aided transcription CATS prior to maskmaking.
DISHING AND TILES

Dishing: large area becomes recessed especially with over polishing

Multiple small dummy features (tiles) are used to reduce Dishing.
Synopsys, Inc. CATS Software for transcription of CAD design files into readable e-beam and laser formats.
RIT ADVANCED CMOS PROCESS

LVL 1 - STI
LVL 2 - NWell
LVL 3 - Pwell
LVL 4 - VTP
LVL 5 - POLY
LVL 6 - PLDD
LVL 7 - NLDD
LVL 8 – N+D/S
LVL 9 – P+D/S
LVL 10 - CC
LVL 11 – METAL 1

NMOSFET
PMOSFET
N+ Poly
P+ Poly
N+ D/S
P+ D/S
n+ well contact
N+ D/S
p+ well contact
P-well
N-well
LDD

N-well
P+ Poly
LDD
n+ well contact

POLY
ACTIVE
P SELECT
CC
METAL
N SELECT
N-WELL

11 PHOTO LEVELS
PARAMETERS THAT AFFECT REMOVAL RATE

Slurry Chemicals
  pH
  Buffering agents
  oxidizers
  complexing agents
  concentration
  dielectric constant

Slurry Abrasive
  type
  size
  concentration
  pH
  suspension stability

Slurry Flow Rate
Films being Polished
Temperature
(5X removal rate/ 20 °C)

Downward Pressure
Platen Speed
Carrier Speed
Pattern Geometries
  Feature Size
  Pattern Density

Pad Type
  fiber structure
  pore size
  hardness
  elastic and shear modulus
  thickness
  embossing or perforations
  conditioning
  aging effects
  chemical durability

Wafer size
CHANGE AND EFFECT

Increase pressure – increase removal rate, degrade surface finish
Increase carrier speed – increase removal rate, degrade uniformity
Increase platen speed – increase removal rate, degrade uniformity
Increase slurry flow – decrease removal rate, improve surface finish
ENDPOINT DETERMINATION METHODS

Calculated Time from Measured Rate
Frictional Force Change – Motor Current
Temperature of Pad
Chemical Indicator
Electrochemical Potential
In-situ Thickness Measurement
Polish Stop Layers, Selectivity
SUMMARY

§ CMP is widely accepted now, after the industry overcame the old paradigm of always keeping the wafer clean.

§ CMP adds cost, ($7-10 per wafer) but its ability to enhance other processing steps while improving circuit performance results in a significant overall benefit.
REFERENCES

Visit your CMP area or interview a CMP expert and determine:

1. Type of equipment used.
2. How endpoint is determined.
3. What pads and slurry are used.
4. When are the pads replaced.
5. What different processes are done. (e.g. what is different when CMP oxide, CMP metal, etc.)