Packaging and Assembly Technology

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OUTLINE

Materials
Terminology and Acronyms
Types of Packages
Processes
Wafer Sawing
Die Bonding
Wire Bonding
Encapsulation
Testing
Reverse Packaging
Costs
### COEFFICIENTS OF THERMAL EXPANSION

#### PACKAGING MATERIALS

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Expansion</th>
<th>Youngs Modulus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicone Elastomers</td>
<td>275-300 ppm/°C</td>
<td></td>
</tr>
<tr>
<td>Unfilled Epoxies</td>
<td>100-200</td>
<td></td>
</tr>
<tr>
<td>Filled Epoxies</td>
<td>50-125</td>
<td></td>
</tr>
<tr>
<td>Epoxy, glass laminates</td>
<td>100-200</td>
<td></td>
</tr>
<tr>
<td>Epoxy, glass laminate, xy axis</td>
<td>12-16</td>
<td></td>
</tr>
<tr>
<td>Aluminum</td>
<td>20-25</td>
<td></td>
</tr>
<tr>
<td>Copper</td>
<td>15-20</td>
<td></td>
</tr>
<tr>
<td>Alumina Ceramic</td>
<td>6.3</td>
<td></td>
</tr>
<tr>
<td>Type 400 Steels</td>
<td>6.3-5.6</td>
<td></td>
</tr>
<tr>
<td>Glass Fabric</td>
<td>5.1</td>
<td></td>
</tr>
<tr>
<td>Borosilicate Glass</td>
<td>5.0</td>
<td>9.1E6 lb/in2</td>
</tr>
<tr>
<td>Silicon</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td>Inconel</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td>Nickel-iron alloy (30 Ni - 61 Fe)</td>
<td>1.22</td>
<td></td>
</tr>
<tr>
<td>Quartz</td>
<td>0.3</td>
<td></td>
</tr>
</tbody>
</table>
### SOLDER

<table>
<thead>
<tr>
<th>Composition</th>
<th>Solidus</th>
<th>Liquidus</th>
</tr>
</thead>
<tbody>
<tr>
<td>70Sn/30Pb</td>
<td>183 °C</td>
<td>193 °C</td>
</tr>
<tr>
<td>63Sn/37Pb</td>
<td>183</td>
<td>183</td>
</tr>
<tr>
<td>60Sn/40Pb</td>
<td>183</td>
<td>190</td>
</tr>
<tr>
<td>50Sn/50Pb</td>
<td>183</td>
<td>216</td>
</tr>
<tr>
<td>40Sn/60Pb</td>
<td>183</td>
<td>238</td>
</tr>
<tr>
<td>10Sn/75Pb</td>
<td>268</td>
<td>302</td>
</tr>
<tr>
<td>42Sn/58Bi</td>
<td>138</td>
<td>138</td>
</tr>
<tr>
<td>70In/30Pb</td>
<td>160</td>
<td>174</td>
</tr>
<tr>
<td>70Sn/18Pb/12In</td>
<td>162</td>
<td>162</td>
</tr>
<tr>
<td>90Pb/5In/2.5Ag</td>
<td>300</td>
<td>310</td>
</tr>
<tr>
<td>97.5Pb/2.5Ag</td>
<td>303</td>
<td>303</td>
</tr>
</tbody>
</table>
Printable solder paste. Paste composition: solder alloy powder, vehicle system (solvents) and flux system.

Printing Techniques: Fine dot dispensing, screen printing, stencil printing. (stencil thickness ~150 µm)

Can be reflowed in air or nitrogen

The flux residues are harmless and can remain on the board without cleaning.
CONDUCTIVE AND NON CONDUCTIVE EPOXY

Non conductive epoxy used to hold chip in place. Epoxy forms a dam and a different type of epoxy fills and protects.

Conductive epoxy is printed, chips are placed on board (tacky epoxy holds them in place), oven cure of epoxy. Conductive epoxy is used where electrical or thermal conductivity is needed.
ADHESIVES

Thermoplastic
Elastomer
Ceramic
Cyanoacrylate
PLASTICS AND POLYMERS

Thermosetting Plastics (Alkyds, Allyls, Epoxies, Phenolics, Polyesters, Polyimides, Polyurethanes)
Thermoplastics Plastics (Acrylics, Fluoropolymers, Liquid Crystal Polymers, Nylons, Polycarbonates, Polyesters, Polyarylates, Polyetherimides, Polyethylene and Polypropylene, Polyimide, Polyamide-Imide, Polyetheretherketones, Polyphenylene Oxide, Polyphenylene Sulfide, Polystyrene, Polysulfone, Polyvinyl Chloride)
Elastomers (Natural Rubber, Acrylic Elastomer, Neoprene, Polyvinyl Chloride Copolymers, Silicone Elastomers, Polyurethanes)
Glass is used to seal lids on packages, form insulation for metal pins into packages.

<table>
<thead>
<tr>
<th>Glass Type</th>
<th>Working Temp °C</th>
<th>Thermal Expansion ppm/°C</th>
<th>Thermal Conductivity W/m K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Borosilicate</td>
<td>1115</td>
<td>46</td>
<td>2</td>
</tr>
<tr>
<td>Lead Glass</td>
<td>560</td>
<td>84</td>
<td></td>
</tr>
<tr>
<td>Silica Glass</td>
<td>1580</td>
<td>5.5</td>
<td>1.6</td>
</tr>
<tr>
<td>Soda Lime Glass</td>
<td>1005</td>
<td>92</td>
<td></td>
</tr>
</tbody>
</table>
## CERAMIC

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Expansion ppm/°C</th>
<th>Thermal Conductivity W/m K</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlN</td>
<td>2.7</td>
<td>150</td>
</tr>
<tr>
<td>Alumina Al2O3</td>
<td>6.3</td>
<td>40</td>
</tr>
<tr>
<td>Beryllia BeO</td>
<td>7</td>
<td>300</td>
</tr>
<tr>
<td>BN</td>
<td>3.8</td>
<td>60</td>
</tr>
</tbody>
</table>
### METALS

<table>
<thead>
<tr>
<th>Metal</th>
<th>Thermal Expansion ppm/°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>22</td>
</tr>
<tr>
<td>Copper</td>
<td>17</td>
</tr>
<tr>
<td>Gold</td>
<td>14.1</td>
</tr>
<tr>
<td>Nickel</td>
<td>13</td>
</tr>
<tr>
<td>Silicon</td>
<td>2.4</td>
</tr>
<tr>
<td>Stainless</td>
<td>17.3</td>
</tr>
<tr>
<td>Inconel</td>
<td>2.4</td>
</tr>
</tbody>
</table>

TO Packages
DIP - Dual In-line Package (PDIP - Plastic DIP)
CERDIP - Ceramic DIP
Ceramic Side Brazed DIP
QFP - Quad Flat Package (MM - Multilayered, Bumpered, HD - High Density)
CLCC - Ceramic Leadless Chip Carrier
CQFP - Ceramic Quad Flat Pack
PQFP - Plastic Quad Flat Pack
SIP - Single In-line Package
MCM - Multi-Chip Module
CSP - Chip Scale Packages (refers to size of package ~ size of chip)
TERMINOLOGY AND ACRONYMS

BGA - Ball Grid Array
PBGA - Plastic Ball Grid Array (or PLGA Plastic Land Grid Array)
PGA - Pin Grid Array
SOT - Small Outline Package
TSOT - Thin Small Outline Package
TCP - Tape Carrier Package (or COT - Chip on Tape)
PACKAGE TYPES

- DIP - (Shrink DIP, CSIP, PDIP, Skinny DIP)
- SIP - Single In-line
- MCM - Multichip Module
- PGA - Pin Grid Array
- Ball Grid Array (PBGA)
- SOP - Small Outline Package (Gull-leaded, J-leaded, TSOP)
- Flat Pack (Quad Flat Pack, Plastic QFP, Ceramic)
- Leadless Chip Carrier
- Leaded chip Carrier
- Tape Automated Bonding
DIP - Dual In Line Packages

- 0.10 inch adjacent pin spacing
- 0.3, 0.4, 0.6, 0.9 inch row spacing
包装和组装

SIP - 单行引脚包

0.10 英寸相邻引脚间距
TO FAMILY OF PACKAGES
QUAD FLAT PACK (QFP)

QFB - Quad Flat Package, leads on all four sides
BQFP - Bumpered
MQFP

Pitch Spacings
1.0 mm
0.8 mm
0.5 mm
0.4 mm
MCM
PGA

Typical 0.10 inch adjacent pin spacing
BALL GRID ARRAY

PBGA-1

PBGA-2

Top side

Ball grid array (BGA)

Solder ball side

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SOLDER BALLS

Alpha Metals
500,000 Spheres
63%Sn/37%Pb

2”
290 gms
BALL GRID ARRAY

Balls are placed on the chip by a machine. The sphere placer is the tool used to place the solder spheres onto the substrate technologies (ball grid array). The spheres are lead and tin, usually with a little silver (referred to as eutectic). There are no-lead solder spheres and other spheres that have different compositions. In the past hi-lead (90% lead, 10% tin) was used. The spheres are anywhere from 12mil to 30mil in size.

One specific tool (Vanguard 5020) is the premier tool in the industry. It works by gravity placement. Flux is placed on the product (which is held in a fixture with vacuum) by screen printing. On the same equipment with a simple rotation of the main fixture the spheres are placed using a stencil. The solder spheres roll into the stencil and then are dropped onto the spots on the part where flux has now been placed. It's phenomenal, the equipment can place upwards of 10,000 spheres in 60seconds or less!
Controlled-Collapse Chip Connections (C4)

The C4 process typically is based on aluminum die pad with sputtered nickel-copper or evaporated chromium-copper and electroless nickel for the Under Bump Metal layers. The bumps themselves are created in a large number of ways. High-melting (~300°C) solders, often with high lead content, which when melted form a bump from the inherent surface tension of solder.
C4 FLIP CHIP

Flip chip has the highest density of interconnects. Example: P2SC single-chip RISC 6000 processor has 2050 C4 bumps on 18x18 mm.
C4 SOLDER BUMP

Final Metal Pad

Solder Bump

Die Passivation

Under Bump Metallurgy

Silicon Wafer

FCT bump structure
C4 SOLDER BUMP FORMATION

1. Silicon wafer with aluminum metal pad and passivation.
2. Under Bump Metallurgy of Cr/Ni/Cu is sputtered.
3. Pattern and Etch to form under bump metal cap.
4. Screen print solder paste and reflow to form bump.

[Image: Printed Bump and Reflowed Bump]
C4 SOLDER BUMP FORMATION

After Printing  →  After Reflow

Close Up of Bump

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C4 FLIP CHIP AFTER ATTACH TO SUBSTRATE
SOLDER BUMPS ON CHIP

- 350 um Solder Bump
- 0.5 um Ni
- 0.1 um Cr
- 1um Al/1%Si

Flip Chip Attach to PCB or Flex Circuit or Tiny Wires
RIT SOLDER BUMP PROCESS

1. Aluminum already on microchip
2. Deposit 1µm of TEOS
3. Photo for etching vias in TEOS (normal positive resist)
4. Etch vias (over etch a little to get undercut for lift-off)
5. Sputter Cr (1000Å), Ni (5000Å) single pump down
6. Sputter Cu (5,000Å) (optional)
7. Lift-Off in acetone using ultrasonic agitation
8. Put down 150µm of the Blue photoresist (negative)
9. Expose and develop openings over the under bump metal
10. Squeegee solder paste filling the openings
11. Heat on hot plate to melt solder and form bumps
12. Solvent strip blue resist off and clean solder flux off
PHOTOSENSITIVE FILMS

http://www.rayzist.com/

Blue Negative Resist

<table>
<thead>
<tr>
<th>Thickness</th>
<th>595 sq in</th>
<th>5 Sheets 8.5” x 14”</th>
<th>1190 sq in</th>
<th>10 Sheets 8.5” x 14”</th>
<th>2975 sq in</th>
<th>25 Sheets 8.5” x 14”</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 mil</td>
<td>$0.063</td>
<td>$37.49</td>
<td>$0.058</td>
<td>$69.02</td>
<td>$0.053</td>
<td>$157.68</td>
</tr>
<tr>
<td>4 mil</td>
<td>$0.068</td>
<td>$40.46</td>
<td>$0.063</td>
<td>$74.97</td>
<td>$0.058</td>
<td>$172.65</td>
</tr>
<tr>
<td>5 mil</td>
<td>$0.073</td>
<td>$43.44</td>
<td>$0.068</td>
<td>$80.92</td>
<td>$0.063</td>
<td>$187.43</td>
</tr>
</tbody>
</table>

Also ImageOn from RIT Bookstore 12”x10’x0.002” thick for $18
IMAGEON ULTRA RAPID DRY FILM RESIST

ImageOn Processing – negative working resist, 50µm Thick

**Wet Substrate**
- Remove mylar film from the non-shiny side of the resist
- Place resist on the wet substrate
- Remove water from center to edge,
  - Laminate or heat on hot plate with pressure
- Remove top mylar film
- Repeat to get 100, 150, 200 µm total thickness

**Expose:**
- Dose = ~50 mj/cm²,
  - Irradiance = 3.5mW/cm² x 15 sec
    - 30s for 100µm, 45s for 150µm, etc.

**Remove top mylar film**
- Develop in CD26 (develop 15 sec, spray DI water, repeat every 15 sec until clear)
- Rinse with water and dry
- Hard bake or expose to UV light for 2 min.
PROCESS DETAILS

Completed CMOS wafer with Al Metal

Deposit 1µm TEOS or LTO

Over etch to create undercut

Deposit Cr and Ni

Lift-Off in Acetone and ultrasonic
PROCESS DETAILS

Apply and Image 150µm Thick Neg. Photoresist

Squeege Fill with Solder Paste

Hot Plate Heat to form Bumps

Solvent Strip 150µm Photoresist
MASK LAYOUT FOR TRIAL SOLDER BUMPS
Pictures During Process

After Imaging 150µm Resist Over Under Bump (Cr/Ni) Metal

After Stripping Resist in Solvent Strip

1mm space, 350 µm Diameter Bump

After Spreading Solder Paste into holes and heating to form Solder Balls
SOLDER PASTE
SEM PICTURES
Polymer Flip Chip Corporation (Billerica, Mass) uses conductive epoxy bumps instead of solder. They use a printing technology to print bumps as small as 75 μm in diameter and 40 μm high. Polymer bumping allows lower temperature processing for a variety of substrates including low temperature, low cost substrates such as mylar, polyester or polycarbonate. If high temperature is needed thermoset polymer bumps are available. An epoxy underfill can be used to provide strength.
SMALL OUTLINE PACKAGE

0.050 inch adjacent pin spacing
SMALL OUTLINE PACKAGE

“J” Leads, Gull Wing, Butt-leaded

0.050 inch adjacent pin spacing
CHIP CARRIER

0.040 and 0.050 inch adjacent pin spacing
ASSEMBLY
WAFER SAWING
DICING SAW BLADES FOR WAFERS, GLASS AND CERAMIC

Resin-bonded dicing blades are made of epoxy with diamond grit for cutting glass, ceramic, pzt, sapphire, etc. Thermocarbon Inc., 391 Melody Lane, P.O. Box 181220, Casselberry, Florida 32718-1220, Tel (407) 834-7800 supply a variety of metal and resin bonded blades. We have 2.25M-15B-46Ru7-3 hubless blades and hubs to hold them. The blades are $25.50 each in Qty of 10. The 2.25 is 2 1/4 inch diameter, the 15 is 0.015 in thick, the 46 is the diamond grit size in µm. Mike Reeves (800) 523-1946 said that this blade should be good for 1 mm thick glass.

Kulicke and Soffa Industries Inc., Micro-Swiss Division, 2101 Blair Mill Road, Willow Grove, PA 19090 Tel(215)784-6975 make metal bonded and resin bonded dicing blades. Their Resinoid Blades with and without hubs are for cutting glass, ceramics, pzt, sapphire, etc. They also have a wide range of nickel hubless and hub-type blades for silicon and GaAs wafers.
Nitto Denko Corporation (http://www.nitto.com)  
Lintec Corp., Tokyo, Japan  

UV Light Release ADWILL T-5782, 200 mm x 10 m roll  
Extra Sticky, ADWILL G-19, 200 mm x 10 m roll
AFTER SAWING AND REMOVAL OF GOOD CHIPS
DIE ATTACH

DIE

Package or Module

System Board

Epoxy or Conductive Epoxy
1. Wafer is presented to die bonder on blue tacky tape. The tape and frame is stretched to increase the separation between die.
2. The bonder’s vision system captures the streets around the die and aligns wafer in X,Y and theta.
3. A lead frame is picked up (or continuous tape) and indexed to the first location.
4. Epoxy is dispensed onto the frame pad where the chip will be placed. (for chips with leads on top or solder bumps on top no epoxy is dispensed. The chip is placed top side down on the frame and is held in place with a tacky pressure sensitive sites until leads are bonded or solder bumps are reflowed making connection and die attach at the same time)
5. Pre bond inspection by vision system to check for bent or missing lead fingers and excess epoxy. (important for high price chips)
6. The wafer is stepped under a vision system to look for ink dots on bad chips.
7. When a good die is found an ejector pin and vacuum pick-up/bonding tool picks up the die and moves over the lead frame.
8. Die is pressed and “scrubbed” into the epoxy. Placement is especially critical for Ball Grid Array packages
9. Post bond inspection by vision system.
10. Lead frame is indexed to next frame.
11. Die epoxy is cured in batch oven for about 1 hour.
Next the die goes to wire bonding or solder bump reflow or other form of making electrical connection between chip and leads on the lead frame.
CSEM 6100 accelerometer with interface circuitry in a TO8 package
**DIE-TO-PACKAGE INTERCONNECT**

- Wire bond (WB)
- Beam lead (BL)
- Flip chip (FC)
- TAB
- BTAB

**Figure 17.2** Illustrating a two-chip hybrid approach to system partitioning. The accelerometer contains no electronics. All of the electronics is on the ASIC chip. (Source: Motorola; reprinted with permission.)
Large diameter gold wire (10 mil) can be ultrasonically bonded to aluminum pads on chips and then can be soldered into a circuit.

Smaller diameter aluminum wire (3 mil) can be ultrasonically bonded to aluminum chip pads and then to packages.
WIRE BONDING

After die bonding the die goes to wire bonding or solder bump reflow or other form of making electrical connection between chip and leads on the lead frame.
Large diameter gold wire (10 mil) can be ultrasonically bonded to aluminum pads on chips and then can be soldered into a circuit.

Smaller diameter aluminum wire (3 mil) can be ultrasonically bonded to aluminum chip pads and then to packages.

12/7/95 RIT purchased 107 feet of 0.010 inch diameter gold wire 4/9’s pure, Hard as Drawn, for wire bonding from Semiconductor Packaging Materials Co., Inc., 431 Fayette Ave., Marmaroneck, NY 10543, tel (914)698-5353, fax (914)698-5386 We had trouble bonding so we called and they said they could anneal the wire to make it softer. We sent it back and they annealed it and it did seem to work better.
Fixture to hold TO-8 and TO-39 packages for wire bonding.
PULL TESTER
Injection Molded
Pre Molded
ENCAPSULATION
HERMETIC SEAL

Hermetic packages prevent water from reaching the integrated circuit. Only metal and ceramic packages are hermetic. Plastic packages are much less expensive but will allow water to quickly penetrate to the integrated circuit. Humidity (water vapor) accelerates corrosion and can cause metallization failure.
Testing of the seal integrity of Hermetic packages are called leak tests. Packages are first tested for gross leaks by immersing in hot flouroinert liquids and looking for bubble escaping from the package as the gas inside expands due to the increase in temperature.
FINE LEAK TEST

If the package passes the gross leak test it is given the helium leak test. The packaged devices are placed in a chamber that can withstand 2000 psi. The chamber is evacuated then back filled with Helium at 2000 psi. and left for 1 hour. Any leaking packages will be filled with Helium. The packages are removed and placed in a chamber attached to a Helium leak detector. As the leak detector pumps on the chamber it can detect Helium from packages that have leaks.
ETCHING THE DUAL-IN-LINE PLASTIC PACKAGE OFF OF PACKAGED CHIPS (DECAPSULATING)

Hot $\text{H}_2\text{SO}_4$ will etch the plastic package and not etch the metal wire bonds or other metal parts as long as no water is present. Straight $\text{H}_2\text{SO}_4$ heated to 100 C for 3 hours to remove all water. Allow to cool to 80C. This etch will remove a plastic package in 30 minutes. Immerse briefly in room temperature $\text{H}_2\text{SO}_4$ to cool the part, then rinse in DI water.
**COSTS**

Costs are from $2 each to $40 each for metal or ceramic packages.

Injection molded packages can be less than $1 each.
REFERENCES

5. Indium Corporation of America, 1676 Lincoln Ave., Utica, NY 13502, Tel (315) 768-6400
1. What does C4 stand for and what is the advantage of this type of connection technology.